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Paper 11
Date: June 24, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE OFFICE OF THE UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLE, INC.,
Petitioner,

v.

WECREVENTION, INC.,
Patent Owner.

IPR2026-00239 (Patent 9,164,942 B2)
IPR2026-00240 (Patent 9,201,834 B2)
IPR2026-00241 (Patent 10,998,017 B2)
IPR2026-00242 (Patent 11,894,098 B2)
IPR2026-00243 (Patent 12,154,652 B2)

Before JOHN A. SQUIRES, *Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office*.

DECISION
Denying Institution of *Inter Partes* Review

WeCrevention, Inc. ("Patent Owner") filed a request for discretionary denial (Paper 7, "DD Req.") in the above-captioned cases, and Apple, Inc. ("Petitioner") filed an opposition (Paper 8, "DD Opp.").[1] On June 12, 2026, after considering the parties' arguments and the record, and in view of all relevant considerations, I issued a Notice indicating that institution is denied in the above-captioned cases. Paper 10.

In IPR2026-00239 and IPR2026-00240, Petitioner affirmatively states that "[a]ll claim terms should be construed according to their ordinary and customary meaning," and that "*no claim terms need be construed* to resolve issues of controversy in the present Petition." Paper 2, 4 (emphasis added). Petitioner also states, as part of its analysis of the challenged claims, that "Petitioner *does not concede that the preambles of the Challenged Claims are limiting*." *Id.* at 9 n.5 (emphasis added).

In district court, however, Petitioner tells a different story, arguing there that the preamble is limiting. Ex. 2016, 6, 7, 9, 12. Indeed, Petitioner specifically denotes that "[r]eview of 'the entirety of the patent' makes clear that the preamble phrase 'high speed memory chip module' contains the core of what the inventors 'actually invented and intended to encompass by the claims,' . . . and *so the preamble should be limiting*." *Id.* at 7 (internal citations omitted, emphasis added).

[1] Unless otherwise noted, citations are to papers in IPR2026-00239. The parties filed similar papers in IPR2026-00240, IPR2026-00241, IPR2026-00242, IPR2026-00243.

Patent Owner contends that Petitioner's assertions about the preamble of the challenged claims are contrary to the holding in *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20 (Director Nov. 3, 2025) (precedential) ("*Revvo*"). Paper 9, 9–10. I agree.

As I have indicated previously, petitioners should be presenting a single construction and applying that construction consistently. *See Infineon Techs. Americas Corp. v. Mosaid Techs. Corp.*, IPR2025-01456, Paper 27 at 3–4 (Director Mar. 17, 2026). Failure to do so, without adequate explanation, is problematic and raises concerns of strategic litigation behavior spill-over into the PTAB inconsistent with Congress's intent to provide a quick and cost-effective alternative to district court litigation. *Id.*; *Revvo*, Paper 20 at 3–4; *see* H.R. Rep. No. 112-98 at 48 (2011). Here, Petitioner offers no explanation for its divergent positions.

Petitioner's positions in IPR2026-00241, IPR2026-00242, and IPR2026-00243 are similarly problematic. In its Petitions, Petitioner identifies "input/output unit" as a means-plus-function limitation and identifies the corresponding structure as input/output unit 106 in the challenged patent. *See, e.g.*, IPR2026-00241, Paper 2, 4. Petitioner also asserts "the applied prior art anticipates or renders obvious the Challenged Claims, regardless of whether 'input/output unit' is construed as a §112(f) means-plus-function limitation," and that "Petitioner is *not conceding* . . . that the '017 Patent provides adequate structure for the 'input/output unit.'" *Id.* at 5 (emphasis added).

In District Court, however, Petitioner once again takes a different position, arguing that the claim term "input/output unit" should be construed as a means-plus-function limitation, identifying the function as "performing input and/or output functions with respect to memory," and asserting that the challenged patent "[l]acks sufficient structure (indefinite)." IPR2026-00241, Ex. 2016, 12. According to Petitioner, "[t]he specification fails to disclose sufficient corresponding structure for performing input and output operations with respect to memory, much less for performing those operations within any particular voltage range." *Id*. at 19.

Petitioner fails to adequately explain its different positions here before the Board and those it propounds in district court. *See, e.g.*, IPR2026-00241, Paper 9. Patent Owner well states the issue; that "[t]o the extent § 112(f) governs, then either input/output unit 106 *is* sufficient corresponding structure (in which case [Petitioner's] district-court indefiniteness argument fails), or it is not (in which case [Petitioner's] IPR mapping relies on a structure [Petitioner] itself maintains is inadequate)." IPR2026-00241, Paper 8, 8–9. I agree. Petitioner's statement that it does not concede the challenged patent provides adequate structure for the "input/output unit" thus only compounds the problem.

While certain arguments are highlighted above, the determination to exercise discretion to deny institution is based on the complete record and a holistic assessment of all of the evidence in light of the arguments presented.

In consideration of the foregoing, it is:

ORDERED that the Petitions are *denied*, and no trial is instituted.

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