Public Version

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN GRAPHIC SYSTEMS, COMPONENTS THEREOF, AND CONSUMER PRODUCTS CONTAINING THE SAME**	**Inv. No. 337-TA-1044**

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Administrative Law Judge MaryJoan McNamara

(April 13, 2018)

Appearances:

For the Complainants Advanced Micro Devices, Inc. and ATI Technologies ULC:

Michael T. Renaud, Esq., James M. Wodarski, Esq., Michael J. McNamara, Esq., William A. Meunier, Esq., Adam S. Rizk, Esq., Marguerite McConihe, Esq., and Cheung Xu, Esq. of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Boston, MA.

Aarti Shah, Esq. of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Washington, D.C.

For the Respondent VIZIO, Inc.:

Cono A. Carrano, Esq., David C. Vondle, Esq., Ryan S. Stronczer, Esq. of Akin Gump Strauss Hauer & Feld LLP, Washington, D.C.

Paul Lin, Esq., Kevin G. McBride, Esq., Brock F. Wilson, Esq., Yimeng Dou, Esq., and Clark Gordon, Esq. of Akin Gump Strauss Hauer & Feld LLP, Irvine, CA.

John Wittenzellner, Esq. of Akin Gump Strauss Hauer & Feld LLP, Philadelphia, PA.

For the Respondents MediaTek Inc. and MediaTek U.S.A. Inc.:

Tyler T. VanHoutan, Esq. of McGuire Woods LLP, Houston, TX.

Rachelle H. Thompson, Esq. of McGuire Woods LLP, Raleigh, NC.

Lyle D. Kossis, Esq. and George B. Davis, Esq. of McGuire Woods LLP, Richmond, VA.

For the Respondent Sigma Designs, Inc.:

Tyler T. VanHoutan, Esq. of McGuire Woods LLP, Houston, TX.

Rachelle H. Thompson, Esq. of McGuire Woods LLP, Raleigh, NC.

Rebecca B. Levinson, Esq. of McGuire Woods LLP, Washington, DC.

Lyle D. Kossis, Esq. and Justin R. Lowery, Esq. of McGuire Woods LLP, Richmond, VA.

Kevin P. Anderson, Esq., Floyd B. Chapman, Esq., and Asia Arminio, Esq. of Wiley Rein LLP, Washington, DC.

For the Commission Investigative Staff:

Margaret D. McDonald, Esq., Director; David O. Lloyd, Esq., Supervisory Attorney; and Yoncha L. Kundupoglu, Esq., Investigative Attorney, of the Office of Unfair Import Investigations, U.S. International Trade Commission, Washington, D.C.

SELECTED SUMMARY FINDINGS

Pursuant to the Notice of Investigation, 82 Fed. Reg. 14748, dated March 22, 2017, this is the Initial Determination ("ID") of the Investigation in the Matter of Certain Graphic Systems, Components Thereof, and Consumer Products Containing the Same, United States International Trade Commission Investigation No. 337-TA-1044. *See* 19 C.F.R. § 210.42(a).

It is a finding of this ID that Advanced Micro Devices, Inc. and ATI Technologies ULC (collectively, "AMD" or "Complainants") have proven by a preponderance of evidence that Respondent VIZIO, Inc. ("Respondent VIZIO") has violated subsection (b) of Section 337 of the Tariff Act of 1930, in the importation into the United States, the sale for importation, or the sale within the United States after importation of consumer products containing certain graphic systems and components thereof.

It is a finding of this ID that Respondent VIZIO has infringed asserted claims 1-5 and 8 of U.S. Patent No. 7,633,506 ("the '506 patent"). It is also a finding of this ID that Respondent VIZIO has not infringed asserted claims 1 and 3 of U.S. Patent No. 7,796,133 ("the '133 patent").

It is a finding of this ID that Complainants have proven by a preponderance of evidence that Respondents MediaTek Inc. and MediaTek U.S.A. Inc. (collectively, "Respondent MediaTek") have violated subsection (b) of Section 337 of the Tariff Act of 1930, in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain graphic systems and components thereof.

It is a finding of this ID that Respondent MediaTek has infringed asserted claims 1-5 and 8 of the '506 patent. It is also a finding of this ID that Respondent MediaTek has not infringed asserted claims 1 and 3 of the '133 patent.

It is a finding of this ID that Complainants have proven by a preponderance of evidence that Respondent Sigma Designs, Inc. ("Respondent SDI," and with Respondent VIZIO and Respondent MediaTek, "Respondents") has violated subsection (b) of Section 337 of the Tariff Act of 1930, in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain graphic systems and components thereof.

It is a finding of this ID that Respondent SDI has infringed asserted claims 1-5 and 8 of the '506 patent. It is also a finding of this ID that Respondent SDI has not infringed asserted claims 1 and 3 of the '133 patent.

It is finding of this ID that Respondents have not proven by clear and convincing evidence that claims 1-5 and 8 of the '506 patent and claims 1 and 3 of the '133 patent are invalid under 35 U.S.C. § 102 as anticipated and/or under 35 U.S.C. § 102 as obvious.

It is a finding of this ID that one or more of Complainants' domestic industry products have satisfied the technical industry prong of the domestic industry requirement for the '506 and '133 patents. It is also a finding of this ID that Complainants have satisfied the economic prong of the domestic industry requirement under Section 337(a)(3)(A), (B), and/or (C).

TABLE OF CONTENTS

ABBREVIATIONS

The following shorthand references to the parties and related U.S. agencies are used in this Initial Determination:

Complainants or AMD	Complainants Advanced Micro Devices, Inc. and ATI Technologies ULC, collectively
Respondent VIZIO	Respondent VIZIO, Inc.
Respondent MediaTek	Respondents MediaTek Inc. and MediaTek U.S.A. Inc., collectively
Respondent SDI	Respondent Sigma Designs, Inc.
Respondents	Respondent VIZIO, Respondent MediaTek, and Respondent SDI, collectively
Staff	Commission Investigative Staff, Office of Unfair Import Investigations
CBP	U.S. Customs and Border Protection
PTO	U.S. Patent and Trademark Office
PTAB	Patent Trial and Appeal Board of the PTO

The following abbreviations for pleadings, exhibits, briefs, transcripts, and Orders are used in this Initial Determination:

Compl.	Complaint
Am. Compl.	Verified Amended Complaint
VIZIO Resp.	Response of Respondent VIZIO to the Notice of Investigation and Complaint Under Section 337 of the Tariff Act of 1930, as Amended
MediaTek Resp.	Response of Respondent MediaTek to the Notice of Investigation and Complaint Under Section 337 of the Tariff Act of 1930, as Amended

SDI Resp.	Response of Respondent SDI to the Notice of Investigation and Complaint Under Section 337 of the Tariff Act of 1930, as Amended
CX	Complainants' exhibit
CDX	Complainants' demonstrative exhibit
CPX	Complainants' physical exhibit
CPBr.	Complainants' Pre-Hearing Brief
CBr.	Complainants' Initial Post-Hearing Brief
CRBr.	Complainants' Post-Hearing Reply Brief
CPSt.	Complainants' Pre-Hearing Statement
JX	Joint exhibit
RX	Respondents' exhibit
RDX	Respondents' demonstrative exhibit
RPX	Respondents' physical exhibit
RPBr.	Respondents' Pre-Hearing Brief
RBr.	Respondents' Initial Post-Hearing Brief
RRBr.	Respondents' Post-Hearing Reply Brief
RPSt.	Respondents' Pre-Hearing Statement
SPBr.	Commission Investigative Staff's Pre-Hearing Brief
SBr.	Commission Investigative Staff's Initial Post-Hearing Brief
SRBr.	Commission Investigative Staff's Post-Hearing Reply Brief
SPSt.	Commission Investigative Staff's Pre-Hearing Statement
Pre-Hearing Tr.	Transcript from November 20, 2017 Pre-Hearing Teleconference (Doc. ID No. 629904 (Nov. 28, 2017))

SX	Staff's exhibit
Tr.	Evidentiary hearing transcript
Dep. Tr.	Deposition transcript
Comp'ls Claim Br.	Complainants' Claim Construction Brief
Res'pts Claim Br.	Respondents' Claim Construction Brief
Staff Claim Br.	Commission Investigative Staff's Claim Construction Brief
***Markman* Hearing Tr.**	Transcript from August 8, 2017 *Markman* hearing (Doc. ID Nos. 619465, 619466 (Aug. 9, 2017))
***Markman* Tutorial Tr.**	Transcript from August 8, 2017 technology tutorial held prior to the *Markman* hearing (Doc. ID No. 619464 (Aug. 9, 2017))
***Markman* Order Tr.**	Transcript from November 8, 2017 oral *Markman* Order (Doc. ID No. 629745 (Nov. 22, 2017))

The following abbreviations for technical business-related terms are used in this Initial Determination:

ALU	Algorithmic logic unit
FIFO	First in, first out
GPU	Graphics processing unit
HDTV	High-definition television
IC	Integrated circuit
MP	Multicore Processor
PLB	Polygon list builder
RTL	Register transfer language
SoC	System on chip

TRM	Technical reference manual

The following shorthand references to certain products and patents at issue in this are used in this Initial Determination:

'506 patent	U.S. Patent No. 7,633,506
'133 patent	U.S. Patent No. 7,796,133
Asserted Patents	'506 and '133 patents, collectively
Accused Products	Accused VIZIO Products, Accused MediaTek Products, and Accused SDI Products, collectively
Accused VIZIO Products	*See* Appendix A; Chart Nos. 7 and 8
Accused MediaTek Products	*See* Appendix A; Chart Nos. 9 and 10
Accused SDI Products	*See* Appendix A; Chart No. 11
Accused Singlepipe Products	*See* Appendix A; Chart Nos. 7 and 9
Accused Multipipe Products	*See* Appendix A; Chart Nos. 8, 10, and 11
DI Products	DI Single Shader Products and DI Multi Shader Products, collectively
DI Single Shader Products	Bristol Ridge, Carrizo, Iceland, Stoney Ridge, and Raven Ridge (*see also* Appendix B; Chart No. 12)
DI Multi Shader Products	Polaris 10 (Ellesmere), Polaris 11 (Baffin), Polaris 12, Polaris 22, Fiji, Tonga, Vega 10, Vega 12, and Vega 20 (*see also* Appendix B; Chart No. 12)

I. INITIAL DETERMINATION ON VIOLATION OF SECTION 337, AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

A. Technology Comment

We live in a world of astonishing color, size, texture, perspective and shape. For those who remember "black and white" television, the images of the world that the black and white medium presented were not true to what we actually see in the "real world" complexity of three-dimension light, color, texture and shading. That world was monochromatic, and more two-dimensional than three-dimensional. Nonetheless, those black and white images constituted a great leap in a number of technologies.

The graphics processing that is incorporated into the two patents at issue in this Investigation, that is U.S. Patent Nos. 7,633,506 and 7,796,133, represent another phase in the refinement of graphics images we see in the real world and in a virtual world. As users of an array of "smart" devices, we have come to expect, and perhaps take for granted, that the refinement of the color, texture, shape and of the objects we see in the real world will be mirrored automatically in, or transmitted into, our television sets, our smart phones and tablets.

This decision, at least in part, describes some of the technology of the graphics processing that enables us to see with exquisite clarity our three-dimensional world in our smart devices. It is hoped that Section IV.A, "Overview of the Technology," which employs the helpful descriptions and images that were provided by the various experts during the *Markman* Hearing and the pre-hearing tutorial render this very complex technology easier to relate to, and easier to understand.

B. Summary of Findings

A summary of this decision's finding is summarized below.

Chart No. 1: Summary of Findings

Product	Patent	Claims	Determination
Accused Multipipe Products	'506 patent	1-5 and 8	***Violation (claims 1-5 and 8)***: Claims 1-5 and 8 of the '506 patent are valid and infringed by the Accused Multipipe Products.
Accused Singlepipe and Multipipe Products	'133 patent	1 and 3	*No violation*: Claims 1 and 3 are valid but not infringed by the Accused Singlepipe and Multipipe Products.
AMD's DI Products	All Asserted Patents		***Satisfied.*** Complainants' domestic R&D activities with respect to their DI Products satisfy the domestic industry requirement set forth in 19 U.S.C. § 337(a)(3)(A), (B), and/or (C).

II. BACKGROUND

A. Institution and Selected Procedural History.

On January 24, 2017, Advanced Micro Devices, Inc. and ATI Technologies ULC filed a complaint under Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, ("Complaint") alleging infringement of certain claims of U.S. Patent No. 7,633,506 (JX-0001, hereafter "the '506 patent"); U.S. Patent No. 7,796,133 (JX-0003, hereafter "the '133 patent"); and U.S. Patent No. 8,760,454 (hereafter "the '454 patent). (*See, e.g.*, Compl. at ¶¶ 1, 6; Doc. ID

No. 601571 (Jan. 24, 2017).).

On March 2, 2017, Complainants filed an amended Complaint ("Amended Complaint") to include the assertion of certain claims of U.S. Patent No. 9,582,846 (hereafter "the '846 patent") against Respondents.[1] (Am. Compl. at ¶¶ 1, 6; Doc. ID No. 604678 (Mar. 2, 2017).).

The Commission instituted this Investigation pursuant to subsection (b) of Section 337 of the Tariff Act of 1930, as amended, to determine:

> whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain graphics systems, components thereof, and consumer products containing the same by reason of infringement of one or more of claims 1-9 of the '506 patent; claims 1-13 and 40 of the '133 patent; claims 2-5, 6-10, and 11 of the '454 patent; and claims 1-8 of the '846 patent, and whether an industry in the United States exists or is in the process of being established as required by subsection (a)(2) of section 337[.]

82 Fed. Reg. 14748 (Mar. 23, 2017).

The Notice of Investigation ("NOI") names Advanced Micro Devices, Inc. of Sunnyvale, CA and ATI Technologies ULC of Ontario, Canada as complainants ("Complainants"). *See id.* The NOI names, *inter alia*, VIZIO, Inc. of Irvine, CA ("Respondent VIZIO"); MediaTek Inc. of Hsinchu City, Taiwan and MediaTek U.S.A. Inc. of San Jose, CA ("Respondent MediaTek"); and Sigma Designs, Inc. of Fremont, CA ("Respondent SDI," and with Respondent VIZIO and Respondent MediaTek, "Respondents").[2] *Id.*

---

[1] In the cover letter of the Amended Complaint ("Amended Complaint Cover Letter"), Complainants explained that on February 28, 2017, after the original Complaint was filed, the U.S. Patent and Trademark Office ("PTO") issued the '846 patent. (Am. Compl. Cover Ltr. at 1.).

[2] The NOI also named LG Electronics, Inc. of Seoul, Republic of Korea, LG Electronics U.S.A., Inc. of Englewood Cliffs, NJ, and LG Electronics MobileComm U.S.A., Inc. of San Diego, CA ("Respondent LG") as Respondents in this Investigation. 82 Fed. Reg. 14748 (Mar. 23, 2017). On October 20, 2017, an ID issued granting Complainants' termination of this Investigation against Respondent LG. (Order No. 48 (Oct. 20, 2017).). The Commission determined not to review the ID. (Doc. ID No. 628691 (Nov.

The NOI also names the Commission Investigative Staff of the Office of Unfair Import Investigations ("Staff," and collectively, with Complainants and Respondents, "the Parties") as a party in this Investigation. *Id.*

On April 17, 2017, Respondent VIZIO filed a response to the Complaint and NOI ("VIZIO Response"). (Doc. ID No. 608891 (Apr. 17, 2017).). On April 19, 2017, Respondent MediaTek and Respondent SDI each filed a response to the Complaint and NOI ("MediaTek Response" and "SDI Response," respectively). (Doc. ID No. 609023 at Ex. 1 (Apr. 17, 2017); Doc. ID No. 609021 at Ex. 1 (Apr. 17, 2017).). In the VIZIO Response, Respondent VIZIO identified eleven (11) affirmative defenses ("Respondent VIZIO's Affirmative Defenses"). (VIZIO Resp. at 23-29.). In the MediaTek Response, Respondent MediaTek identified twelve (12) affirmative defenses ("Respondent MediaTek Affirmative Defenses"). (MediaTek Resp. at 31-36.). In the SDI Response, Respondent SDI also identified twelve (12) affirmative defenses. (SDI Resp. at 31-36.).

On May 26, 2017, Complainants filed a motion seeking leave to file a second Amended Complaint ("Second Amended Complaint") based on the U.S. Patent and Trademark Office's ("PTO") issuance of a Certificate of Correction under 37 C.F.R. § 1.323 for the '846 patent.[3] (Motion Docket No. 1044-014 (May 26, 2017).). An ID granting Complainants' motion was

---

13, 2017).).

[3] On June 14, 2017, Complainants filed a motion for leave to file a third Amended Complaint ("Third Amended Complaint") to add MStar Semiconductor, Inc. ("MStar"), a wholly-owned subsidiary of MediaTek Inc., as a respondent. (Motion Docket No. 1044-018 (June 14, 2017).). On November 8, 2017, Complainants filed a notice withdrawing their Third Amended Complaint. (Doc. ID No. 628359 (Nov. 8, 2017).). On July 19, 2017, Complainants filed a motion for leave to file a fourth Amended Complaint ("Fourth Amended Complaint") to assert the '454 and '846 patents against Respondent VIZIO. (Motion Docket No. 1044-025 (July 19, 2017).). Complainants' motion for leave to file a Fourth Amended Complaint was denied. (Order No. 32 (Aug. 11, 2017).).

issued. (Order No. 27 (July 25, 2017).). The Commission determined not to review the ID. (Doc. ID No. 619582 (Aug. 10, 2017).).

On August 15, 2017, an ID issued granting Complainants' first partial termination of this Investigation against Respondents with respect to claims 4-6 of the '133 patent. (Order No. 33 (Aug. 15, 2017).). The Commission determined not to review the ID. (Doc. ID No. 622045 (Sept. 5, 2017).). On October 5, 2017, an ID issued granting Complainants' second partial termination of this Investigation against Respondents with respect to claims 9, 10, 11, and 12 of the '133 patent. (Order No. 43 (Oct. 5, 2017).). On October 31, 2017, an ID was issued granting Complainants' third partial termination of this Investigation against Respondents as to the '454 and '846 patents, claims 2, 7, 8, 13, and 40 of the '506 patent, and claims 6, 7, and 9 of the '846 patent. (Order No. 53 (Oct. 31, 2016).). The Commission determined not to review the ID that issued on October 31, 2017. (Doc. ID No. 630055 (Nov. 28, 2017).).

Following the termination of the '454 and '846 patents and certain claims of the '506 and '133 patents, the Asserted Patents and claims remaining that are the subject of this decision are claims 1-5 and 8 of the '506 patent and claims 1 and 3 of the '133 patent.

On August 8, 2017, a *Markman* hearing and a technical tutorial were held. (Doc. ID Nos. 619465, 619466 (Aug. 9, 2017).).

On November 8, 2017, a telephonic conference with regard to claim construction was held ("Claim Construction Teleconference"). During the Claim Construction Teleconference, rulings issued with respect to the level of ordinary skill in the art and the constructions of the disputed claim terms. (*See Markman* Order Tr.).

Complainants filed five (5) motions *in limine* ("MIL"). (Motion Docket Nos. 1044-047

(Oct. 19, 2017), 1044-054 (Nov. 3, 2017), 1044-055 (Nov. 3, 2017), 1044-056 (Nov. 3, 2017),[4] 1044-057 (Nov. 3, 2017).). Respondents filed four (4) MILs and two (2) high-priority objections ("HPO"). (Motion Docket Nos. 1044-050 (Oct. 25, 2017), 1044-058 (Nov. 3, 2017), 1044-059 (Nov. 3, 2017), 1044-060 (Nov. 3, 2017); Doc. ID No. 627936 (Nov. 3, 2017).).[5]

On November 20, 2017, during a telephonic pre-hearing conference ("Pre-Hearing Teleconference"), the following rulings with respect to the Parties' MILs and HPOs were issued. The Parties' MILs and HPOs, and the rulings on these motions/objections, are summarized in Chart Nos. 2 and 3 below.

Chart No. 2: Complainants' MILs

MIL No.	Issue	Ruling
MIL No. 1	Motion to strike portions of Dr. Anselmo Lastra's[6] Expert Report and to preclude testimony at the evidentiary hearing concerning certain late-disclosed non-infringement contentions (Motion Docket No. 1044-047)	Denied, without prejudice. (Pre-Hearing Tr. at 13:3-5.).
MIL No. 2	Motion to preclude late-disclosed and unreliable expert opinion regarding inherency (Motion Docket No. 1044-055)	Granted. (*Id.* at 19:9-19.).
MIL No. 3	Motion to preclude testimony on improperly	Denied, without

[4] Complainants withdrew their MIL No. 4. (*See* Doc. ID No. 628644 (Nov. 13, 2017); Pre-Hearing Tr. at 27:22–28:7.).

[5] Respondents withdrew their HPO No. 1. (*See* Doc. ID No. 628661 (Nov. 13, 2017); Pre-Hearing Tr. at 47:22–48:7.).

[6] When he testified during the evidentiary hearing on November 29, 2017, Dr. Anselmo Lastra was a Professor Emertius at the University of North Carolina, Chapel Hill, in the Department of Computer Science. (RPSt. at 2; *id.* at Ex. 1; Tr. (Lastra) at 704:10-14.). Respondents identified Dr. Lastra as an expert to provide testimony with regard to: (1) the state of the art; (2) claim construction; (3) non-infringement of the asserted claims of the '506 and '133 patents; and (4) rebuttal to any issues and evidence presented by Complainants. (RPSt. at 2.).

MIL No.	Issue	Ruling
	withheld source code (Motion Docket No. 1044-054)	prejudice. (*Id.* at 27:20-21.).
MIL No. 5	Motion to preclude testimony elaborating on claim terms not timely construed by Respondents (Motion Docket No. 1044-057)	Denied. (*Id.* at 31:20–32:4.).

Chart No. 3: Respondents' MILs and HPOs

MIL No./HPO No.	Issue	Ruling
MIL No. 1	Motion to strike portions of Dr. Glenn Reinman's[7] Expert Report and to preclude testimony at the evidentiary hearing concerning the same (Motion Docket No. 1044-050)	Denied. (Pre-Hearing Tr. at 34:18–35:1.).
MIL No. 2	Motion to preclude Dr. Reinman's claim construction opinions with respect to disputed terms and Complainants' reliance on the same (Motion Docket No. 1044-059)	Granted. (*Id.* at 41:19-25.).
MIL No. 3	Motion to preclude certain theories, opinions, and evidence regarding any purported "ALU" and/or "ALU/Memory Pair" in the accused products[8] (Motion Docket No. 1044-060)	Denied, without prejudice. (*Id.* at 44:18-23.).
MIL No. 4	Motion to preclude Complainants from presenting untimely theories, opinion, and evidence not	Denied. (*Id.* at

[7] When he testified during the evidentiary hearing on November 24, 2017, November 28, 2017, and December 1, 2017, Dr. Glenn Reinman was a Professor in the Department of Computer Science and Graduate Vice Chair at the University of California, Los Angeles. (CPSt. at Ex. 1.). Complainants identified Dr. Reinman as an expert to provide testimony with respect to: (1) the technical background of the Asserted Patents and Accused Products; (2) characteristics of a person of ordinary skill in the art; (3) claim construction; (4) infringement of the Asserted Patents; (5) the domestic industry technical prong as to the practice of the Asserted Patents by Complainants' DI Products; and (6) rebuttal of any testimony of Respondents' experts or facts witnesses within his areas of expertise. (*Id.* at 3.).

[8] "ALU" is an acronym for "arithmetic logic unit." (Tr. (Reinman) at 290:10-14; Tr. (Lastra) at 773:3–775:11.). The ALU performs arithmetic and logical operations. (Tr. (Reinman) at 290:10-14; Tr. (Lastra) at 773:3–775:11.).

MIL No./HPO No.	Issue	Ruling
	disclosed in their infringement contentions (Motion Docket No. 1044-058)	47:12-13.).
HPO No. 2	Objection to Complainants' use of Complainants' Exhibit No. CX-04208SC with Dr. Reinman (*id.*)	Granted in-part. (*Id.* at 56:13-22.).

(*Id.*).

The evidentiary hearing was held from November 27, 2017 through December 1, 2017. Complainants alleged that Respondents have infringed the Asserted Patents and claims identified in Chart No. 4, below, which were the focus of testimony during the evidentiary hearing.

Chart No. 4: Patents and Claims at Issue

U.S. Patent No.	Claims Asserted[9]
7,633,506	**1**, 2-5, and 8
7,796,133	**1** and 3

On December 4, 2017, a notice addressing post-hearing briefs and motions ("Post-Hearing Notice") issued. (Doc. ID No. 630562 (Dec. 4, 2017).). The Post-Hearing Notice instructed the Parties to file, *inter alia*, any post-hearing motions by December 22, 2017. (*Id.*; Order No. 24 (July 17, 2017).).

On December 22, 2017, Complainants filed three (3) motions to strike. (Motion Docket Nos. 1044-066 (Dec. 22, 2017), 1044-068 (Dec. 22, 2017), 1044-069 (Dec. 22, 2017).). On the same day, Respondents filed two (2) motions to strike. (Motion Docket Nos. 1044-070 (Dec. 22, 2017), 1044-071 (Dec. 22, 2017).). The Parties' motions to strike, and the rulings on these

[9] Bolded patent claim numbers indicate independent claims.

motions, are summarized in Chart Nos. 5 and 6 below.

Chart No. 5: Complainants' Motions to Strike

Motion Docket No.	Issue	Ruling
1044-066	Motion to strike portions of the hearing testimony of Dr. Anselmo Lastra as outside the scope of his expert report and Respondents' Pre-Hearing Brief	Denied. (Order No. 62 at 2-6 (Apr. 12, 2018).).
1044-068	Motion to strike portions of hearing testimony of Mr. Guy Larri[10] consisting of improper expert testimony by a lay witness	Denied. (*Id.* at 6-10.).
1044-069	Motion to strike portions of the hearing testimony of Dr. Stephen Edwards[11] as outside the scope of his expert report and Respondents' Pre-Hearing Brief	Denied. (*Id.* at 10-12.).

Chart No. 6: Respondents' Motions to Strike

Motion Docket No.	Issue	Ruling
1044-070	Motion to strike testimony of Glenn Reinman and	Denied. (Order No. 62 at 12-13 (Apr. 12,

[10] When he testified during the evidentiary hearing on November 28-29, 2017, Mr. Guy Larri was a [redacted] Respondents identified Mr. Larri as a fact witness to provide testimony with regard to the structure, function and operation of the [redacted] included in certain of Respondents' Accused Products, and rebuttal to any issues and evidence that Complainants present. (RPSt. at 2.).

[11] When he testified during the evidentiary hearing on November 30, 2017 and December 1, 2017, Dr. Stephen Edwards was an Associate Professor at Columbia University, in the Department of Computer Science. (RPSt. at Ex. 2; Tr. (Edwards) at 937:10-15.). Respondents identified Dr. Edwards as an expert to provide testimony on: (1) the state of the art; (2) claim construction; (3) invalidity of the '506 and '133 patents; and (4) rebuttal to issues and evidence presented by Complainants. (*Id.* at 3.).

Motion Docket No.	Issue	Ruling
	related exhibits	2018).).
1044-071	Motion to strike portions of the testimony of Dr. Andrew Wolfe[12]	Denied. (*Id.* at 13-16.).

B. The Parties.

1. Complainants Advanced Micro Devices, Inc. and ATI Technologies ULC ("Complainants" or "AMD")

Complainant Advanced Micro Devices, Inc. is a Delaware corporation with its principal place of business at One AMD Place, Sunnyvale, California 94085. (Compl. at ¶ 9.). ATI Technologies ULC is incorporated in Canada and has its principal place of business at 1 Commerce Valley Drive East, Markham, Ontario L3T 7X6, Canada. (*Id.*). ATI Technologies ULC is a wholly-owned subsidiary of Advanced Micro Devices, Inc.[13] (*Id.*). ATI Technologies ULC is the sole owner by assignment of all right, title, and interest in each Asserted Patent. (*Id.*, Ex. 1 at ¶¶ 4-5; *see also id.* at Exs. 7, 10, 12-13, 16-18.).

AMD is an American multinational semiconductor company that develops and manufactures graphic systems. (*Id.* at ¶ 2.). AMD's semiconductor technology powers intelligent devices, such as personal computers, game consoles, and cloud servers. (*Id.* at ¶ 4.). AMD's technology is also featured inside gaming consoles and laptop computers, including the

[12] When he testified during the evidentiary hearing on December 1, 2017, Dr. Andrew Wolfe was a consultant of Wolfe Consulting and a lecturer at Santa Clara University. (CPSt. at Ex. 2.). Complainants identified Dr. Wolfe as an expert to provide testimony with respect to: (1) the technical background of the Asserted Patents and Accused Products; (2) characteristics of a person of ordinary skill in the art; (3) claim construction; (4) prior art; (5) validity of the Asserted Patents; and (6) rebuttal testimony of Respondents' experts or fact witnesses on matters within his areas of expertise. (*Id.* at 3.).

[13] Advanced Micro Devices, Inc. acquired ATI Technologies ULC in 2006. (Compl. at ¶ 2.).

Microsoft Xbox One, Sony PlayStation, and Apple MacBook Pro. (*Id.*). Additionally, AMD's technology is used to deliver rich interfaces and photorealistic graphics to consumer products such as smartphones, tablets, televisions, and wearable devices. (*Id.*).

2. Respondent VIZIO, Inc. ("Respondent VIZIO")

Respondent VIZIO, Inc. is a California corporation with a principal place of business at 39 Tesla, Irvine, California 92618. (VIZIO Resp. at ¶ 14.). VIZIO, Inc. markets and sells high-definition televisions ("HDTVs"), sound bars and speakers, and accessories. (RBr. at 10.).

3. Respondents MediaTek Inc. and MediaTek U.S.A. Inc. ("Respondent MediaTek")

Respondent MediaTek Inc. is a Taiwanese company and maintains its principal place of business at No. 1, Dusing Road 1, Hsinchu Science Park, Hsinchu City 30078, Taiwan. (MediaTek Resp. at ¶ 15.). MediaTek's business includes designing, developing, and selling system-on-chip ("SoC")[14] products that are and utilized in smartphones, tablets, and televisions. (RBr. at 10.).

Respondent MediaTek U.S.A. Inc. is a wholly-owned subsidiary of MediaTek Inc. (MediaTek Resp. at ¶ 17.). MediaTek U.S.A. Inc. is a Delaware corporation and maintains its principal place of business at 2860 Junction Avenue, San Jose, California 95134. (*Id.*). MediaTek U.S.A. Inc. engages in research and development ("R&D") in the U.S. relating to certain technology. (*Id.*; *see also* RBr. at 10.).

4. Respondent Sigma Designs, Inc. ("Respondent SDI")

Respondent Sigma Designs, Inc. is a domestic corporation with its principal place of

[14] An SoC, or a "system on chip[,] is a variety of components that are integrated onto a single integrated circuit, single piece of silicon, and they have functionality that may be in different processing areas." (Tr. (Reinman) at 161:5-9.).

business at 47467 Fremont Boulevard, Fremont, California 94538. (SDI Resp. at ¶ 18.). Sigma Designs, Inc.'s business includes designing and developing SoC products that are [redacted] and utilized in televisions. (RBr. at 10 *see also* SDI Resp. at ¶ 19.).

III. JURISDICTION, IMPORTATION, AND STANDING

A. The Commission Has Jurisdiction

To have the authority to decide a case, a court or agency must have both subject matter jurisdiction and jurisdiction over either the parties or the property involved. *See Certain Steel Rod Treating Apparatus and Components Thereof*, Inv. No. 337-TA-97, Comm'n Opinion, 215 U.S.P.Q. 229, 231 (U.S.I.T.C. 1981). For the reasons discussed below, the facts support a finding that the Commission has jurisdiction over this Investigation.

1. Subject Matter Jurisdiction

The Commission has subject matter jurisdiction over this Investigation because Complainants alleged that Respondents have violated 19 U.S.C. §1337(a)(1)(B). *See Amgen v. U. S. Int'l Trade Comm'n*, 902 F.2d 1532, 1536 (Fed. Cir. 1990). Respondents have not contested that the Commission has subject matter jurisdiction. (RPBr. at 9; RBr. at 18; SBr. at 13.).

2. Personal Jurisdiction

Respondents have appeared and responded to the Complaint and NOI, and participated in discovery and the evidentiary hearing. Thus, the Commission has personal jurisdiction over these Respondents. *See, e.g., Certain Windshield Wiper Devices and Components Thereof* ("*Wiper Devices*"), Inv. No. 337-TA-881, ID at 5 (May 8, 2014) (unreviewed in relevant-part) (Doc. ID No. 534255).

3. *In Rem* Jurisdiction

Section 337(a)(1)(B) applies to the "[t]he importation into the United States, the sale for importation, or the sale within the United States after importation" of articles that infringe a valid and enforceable United States patent." 19 U.S.C. § 1337(a)(1)(B). A single instance of importation is sufficient to satisfy the importation requirement of Section 337. *Certain Optical Disc Drives, Components Thereof, and Prods. Containing the Same*, Inv. No. 337-TA-897, Order No. 101 at 3 (Sept. 22, 2014) (citations omitted) (EDIS Doc. 543438).

Respondent VIZIO did not dispute that the Accused VIZIO Products are [redacted]. (JX-0010C (Importation and Inventory Stip.) at ¶¶ 3, 6; RPBr. at 9.). Respondent VIZIO stipulated that: [redacted]. (JX-0010C.0020[16] at ¶¶ 2-3, 5-6; CX-3752C.0099 (VIZIO

[15] The Accused VIZIO Products include [redacted] (CX-3752C (VIZIO Resp. to AMD Interrog. No. 2) at 57-71 [redacted]; CX-3848C (MediaTek Resp. to AMD Interrog. No. 2) at 12-14 [redacted]; CX-3872C (SDI Resp. to AMD Interrog. No. 2) at 11-13 [redacted]).

[16] The stipulation identifies [redacted] (*Id.* at ¶ 2.).

Resp. to AMD Interrog. No. 20) ( ); *see also id.* at App. C.).

The record evidence also demonstrates that the Accused MediaTek Products are and that Respondent MediaTek has . (CX-3848C.33-34 (MediaTek Resp. to Interrog. No. 15 ( )); *id.* at 36 (MediaTek Resp. to Interrog. No. 17 ( ).).

Additionally, evidence adduced in this Investigation reflects that Respondent SDI . (*See* CX-3873C.0013-16 (SDI Resp. to Interrog. Nos. 20-21 ( ); CX-4204C.0009-10 (SDI Resp. to RFA Nos. 113, 134 ( ).). In addition, Respondent VIZIO admitted that it . (JX-0010C.0020.).

Thus, evidence presented in this Investigation establishes that the Commission has *in rem* jurisdiction over the Accused VIZIO, MediaTek, and SDI Products. *See, e.g.*, *Wiper Devices*, Inv. No. 337-TA-881, Inv. No. 337-TA-881, Initial Determination at 5 (*in rem* jurisdiction exists when importation requirement is satisfied).

B. Complainants Have Standing in the Commission

Jurisdiction also requires standing. *See SiRF Technology, Inc. v. Int'l Trade Comm'n*, 601 F.3d 1319, 1326 (Fed. Cir. 2016) (standing to bring an infringement suit is the same under

Commission Rules as it would be in a Federal District Court case); *Certain Optical Disc Drives, Components Thereof and Prods. Containing Same*, Inv. No. 337-TA897, Opinion Remanding the Investigation at 4 (Jan. 7, 2015). Commission Rule 210.12 requires that intellectual-property based complaints filed by a private complainant "include a showing that at least one complainant is the exclusive license of the subject intellectual property." 19 C.F.R. § 210.12(a)(7).

Complainants have standing to bring suit for infringement under Section 337 because ATI Technologies ULC is the owner of the Asserted Patents. (Compl., Ex. 1 at ¶¶ 4-5; *see also id.* at Exs. 7, 10, 12-13, 16-18.).

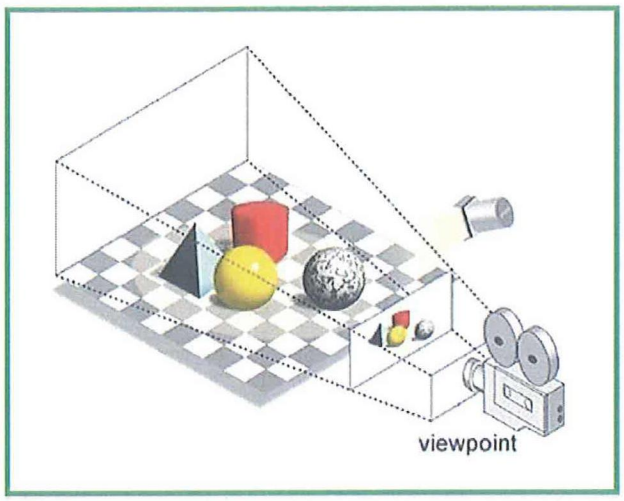
Moreover, because Respondents have not contested Complainants' standing, Respondent MediaTek's Eleventh Affirmative Defense and Respondent SDI's Eleventh Affirmative Defense for lack of standing are deemed by this decision to be waived and abandoned pursuant to Ground Rules 7.2 and 10.1.

IV. THE ASSERTED PATENTS

A. Overview of the Technology

This Investigation generally concerns graphics processing unit circuitry used to convert three-dimensional objects into an image for display on a two-dimensional screen. (Tr. (Reinman) at 158:17–159:11.).

Figure No. 1: Three-Dimensional Objects Displayed on a Two-Dimensional Screen



(CDX.0100C.0004.).

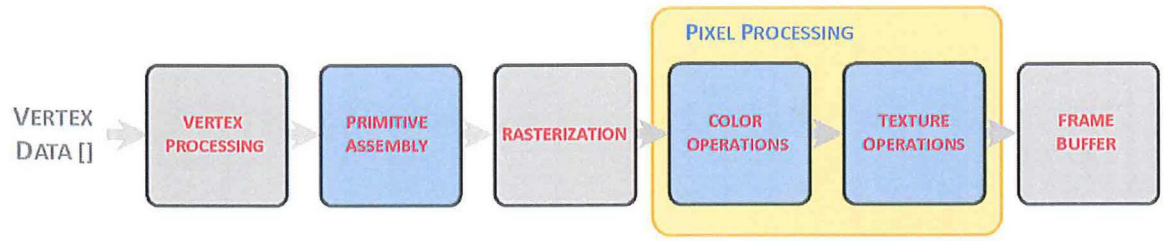
Rendering interactive three-dimensional images onto the two-dimensional screen of a computer or mobile device requires intensive processing capabilities performed by specialized chips called graphics processing units ("GPUs"). (JX-0001 at 2:14-19; *see also Markman* Tutorial Tr. (Wolfe) at 12:20–14:25 ("the graphics processing unit does all of the mathematical calculations that are involved in creating this 3D world and allow to you [sic] visualize this 3D world"); *Markman* Tutorial Tr. (Lastra) at 27:6–28:19; CX-3891C (Reinman Expert Report) at ¶ 38 ("Graphics processing is a difficult problem because it combines a dramatic need for computation that is both fast and flexible. Computers and mobile devices are interactive, requiring the display of dynamically generated scenes.").).

Inside the GPU, the data that is ultimately displayed on a monitor or screen progresses through a "graphics pipeline," which is comprised of a number of processing stages. (*Markman* Tutorial Tr. (Reinman) at 15:1-9 ("Now, we traditionally call the process of creating 3D graphics a graphics pipeline. And the idea is that you start with this general mathematical description of

the world, and you push it through a number of stages to try to get a picture out the other end."); *Markman* Tutorial Tr. (Lastra) at 28:23–29:9 ("[L]et me digress a little bit and tell you why we call it a graphics pipeline. It's because things flow through. It's really more like an assembly line where at each of those boxes, each of these stages, a different job is being done, the same as these workers are doing different things."). The point of the graphics pipeline is to process information at one stage and move it along to the next stage. (Tr. (Wolfe) at 1389:20-25; Tr. (Reinman) at 165:10-15.).

A rudimentary graphics pipeline ("Pipeline") involves the following stages: (1) vertex processing; (2) primitive assembly; (3) rasterization; (4) pixel processing, which includes the application of color and texture; and (5) storing the image in a frame buffer. (*Markman* Tutorial Tr. (Wolfe) at 15:10–20:1; *Markman* Tutorial Tr. (Lastra) at 29:10–32:32.).

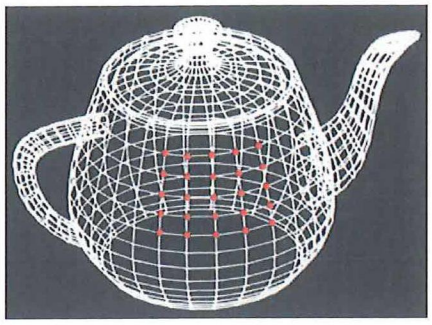
Figure No. 2: Graphics Pipeline



(CDX-0100C.0007.).

As shown above, the Pipeline generally starts with the vertex processing step. (*Markman* Tutorial Tr. (Wolfe) at 15:10-16; CDX-0100C.8; *Markman* Tutorial Tr. (Lastra) at 29:10-19.). A vertex is a point in a coordinate space that is used to define the shape of an object. (*Markman* Tutorial Tr. (Wolfe) at 15:10-12; Tr. (Reinman) at 165:23–166:2; CX-3891C at ¶ 40.).

Figure No. 3: Illustration of a Shape's Vertices

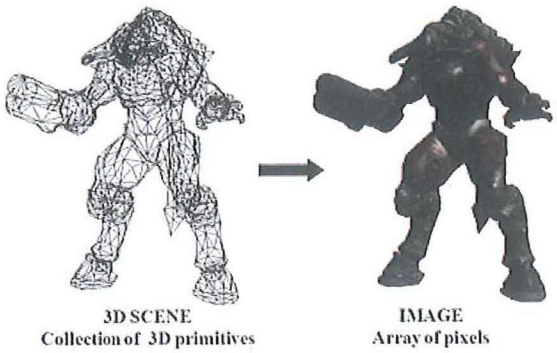


(CDX-0100C.0008.).

These vertices processed during the vertex processing step can be manipulated depending on the type of lighting and the position/orientation of the viewpoint in order to integrate the object into a given scene. (Tr. (Reinman) at 166:4-11; *Markman* Tutorial Tr. (Wolfe) at 15:10–16:10; *Markman* Tutorial Tr. (Lastra) at 29:10-19; CX-3891C at ¶ 40.).

In the primitive assembly step, the vertices are assigned to "primitives" or "simple shapes," which can be in the form of points, lines, or triangles, as seen below. (*Markman* Tutorial Tr. (Wolfe) at 16:11-20; *Markman* Tutorial Tr. (Lastra) at 29:24–30:2; Tr. (Reinman) at 166:12-25; CMX-0001 (Wolfe Decl.) at ¶ 22.). For example, in the figure below, a three-dimensional character has been rendered as a collection of triangular primitives.

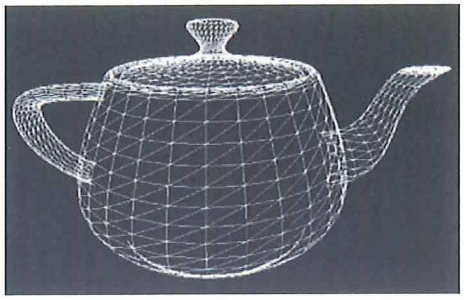
Figure No. 4: Primitives



(Comp'ls Claim Br. at 10.).

For triangular primitives, which are common, each triangular primitive is defined by the positions of its three (3) corner points, i.e., its vertices. (CMX-0001 at ¶ 23; Tr. (Reinman) at 166:17-23.).

Figure No. 5: Illustration of a Shape's Primitives

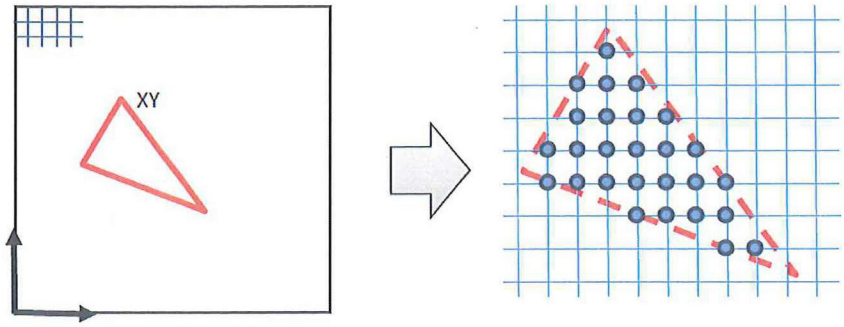


(CDX-0100C.0009.).

After a three-dimensional object is rendered as a group of primitives, during rasterization, the vertices of each primitive is converted from three-dimensional coordinates to two-dimensional coordinates, and each primitive is rendered as a two-dimensional collection of dots called "pixels." (CMX-0001 at ¶¶ 23-24; *Markman* Tutorial Tr. (Wolfe) at 16:21–17:14; Tr. (Reinman) at 167:4-20.).

The graphics processor uses the two-dimensional vertices coordinates to determine which pixels fill a particular primitive. (CXM-0001 at ¶ 24.). In the illustration below, the pixels that fill the primitive defined by the x-y coordinates are depicted as blue dots.

Figure No. 6: Rasterization

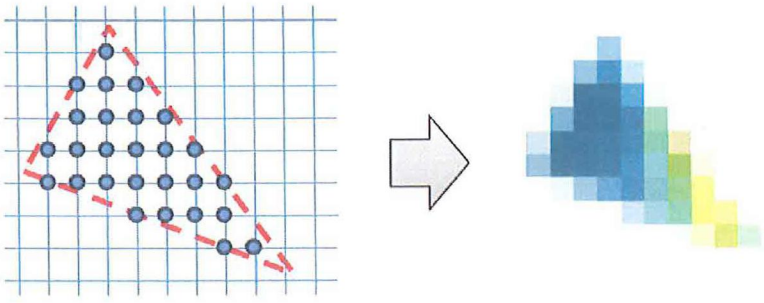


(Comp'ls Claim Br. at 11 (citing CXM-0001 at ¶ 25).).

Once the positions of the pixels are established, they undergo a series of pixel processing steps that involve color and texture operations. (CXM-0001 at ¶ 25; Tr. (Reinman) at 169:1-10; *Markman* Tutorial Tr. (Wolfe) at 17:15–19:20; Tr. (Lastra) at 31:5–33:14; JX-0001 at 1:43-46; JX-0003 at 1:27-29.).

Color operations include assigning each pixel a base color. (CXM-0001 at ¶ 25; *Markman* Tutorial Tr. (Wolfe) at 17:15–19:20.). Additional operations such as lighting and blending may also be performed. (CXM-0001 at ¶ 25; *Markman* Tutorial Tr. (Wolfe) at 17:15–18:1.).

Figure No. 7: Blending

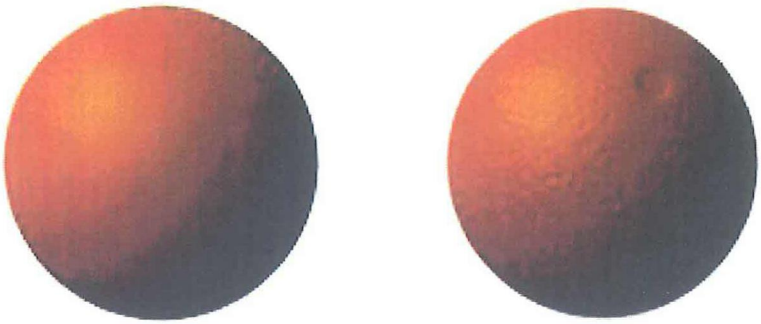


(Comp'ls Claim Br. at 11 (citing CXM-0001 at ¶ 26).).

Texture operations further refine a pixel's color attribute by wrapping predetermined

patterns onto the pixel. (Tr. (Reinman) at 169:19–171:6; Tr. (Wolfe) at 1371:24–1372:7.). Texture operations modify the base color so that the final image appears more realistic, for example, by making the surface of an object appear "bumpy." *Markman* Tutorial Tr. (Wolfe) at 17:18-24, 18:4-25; JX-0003 at 2:20-42.).

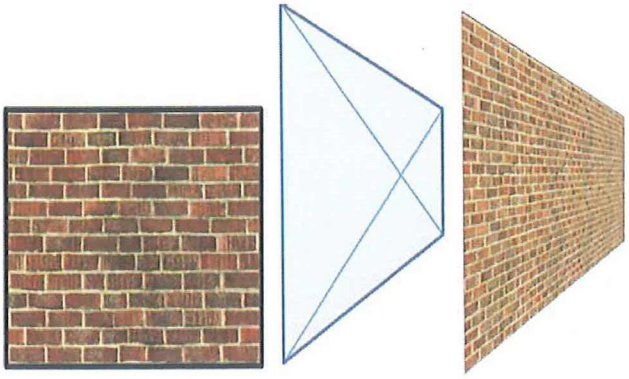
Figure No. 8: Texturing



(CDX-0001.11)

In another example below, a "brick wall" texture is applied to the primitives in a perspective-correct view.

Figure No. 9: Texturing



(CDX-0100C.0013; Tr. (Reinman) at 170:12–171:3.).

Texture mapping refers to a texture operation in which the texture coordinates[17] of the predetermined pattern that are to be applied to a pixel are determined and retrieved. (Tr. (Reinman) at 171:21–172:10 ("[I]n the focus of texturing, [the rasterizer is] generating texture coordinates for those incoming pixels. Now, those texture coordinates are what part of the wallpaper do we want to grab, right. So we go to the texture mapping portion, which is in pink. And the texture unit will take those coordinates and say okay, this is a piece of wallpaper you want. Think of it, you're going to the wallpaper store, you're going to grab a piece of the wallpaper and you're going to put it on a particular location of your primitive. That retrieval is what is texture mapping. You have a coordinate, and you use that to go off to memory and grab data."); CDX-0100C.0013; Tr. (Wolfe) at 1369:12–1370:11, 1372:8-14 ("Texture mapping is simply the process of figuring out which part of a texture corresponds to which pixel we see on the screen. So it's just -- it's this wrapping of textures around objects. It's figuring out what part of the texture we want to see at each spot on the screen.").).

Texture coordinate shading is a more complex texture operation than texture mapping. (Tr. (Reinman) at 172:8-14; CDX-0100C.0015; *see also* Tr. (Wolfe) at 1372:15–1373:2 (texture mapping versus texture coordinate shading). Texture coordinate shading involves modifying texture coordinates after they are generated. (Tr. (Wolfe) at 1377:15–1378:7 (defining texture coordinate shading and providing examples of effects achieved with texture coordinate shading); Tr. (Reinman) at 172:11–173:11 ("But now that we have those texture coordinates per pixel, we can then go into texture coordinate shading at the unified shader and we can refine them, modify

[17] Texture coordinates define the location in a texture map from which texture data can be retrieved for a rasterized pixel during texture mapping. (Tr. (Reinman) at 171:7–172:10; CDX-0100.14.). The rasterizer generates/produces the texture coordinates in the first instance. (Tr. (Reinman) at 172:15–174:7; JX-0001.0021 at 6:38-40; CDX-0100.15, 16; Tr. (Lastra) at 1369:17-20.).

them. There can be arithmetic operations like the one I show on the bottom here, U, which is a coordinate, plus .5, sort of scaling or biasing the particular coordinate. Then what we have at the end of whatever amount of processing is required is a shaded texture coordinate. And that shaded texture coordinate is an input to the texture unit, which would then retrieve that particular portion from texture memory and again we have texture data."), 444:11-20; *see also* JX-0001.002 at 6:43-49 ("A unified shader **570** works in conjunction with the texture unit **585** and applies a programmed sequence of instructions to the rasterized values. These instructions may involve simple mathematical functions (add, multiply, etc.) and may also involve requests to the texture unit. A unified shader reads in rasterized texture addresses and colors, and applies a programmed sequence of instructions.").). An example of texture coordinate shading is the depiction of reflections in irregular objects, such as reflections in a pond in which the water is moving and the reflected texture changes over time. (Tr. (Wolfe) at 1377:15–1378:7.).

B. U.S. Patent No. 7,633,506 ("the '506 Patent")

1. Overview of the '506 Patent

The '506 patent, titled "Parallel Pipeline Graphics System," was filed on November 26, 2003, as U.S. Patent Application Serial No. 10/724,384 ("the '384 application"). (JX-0001 at (21), (22), (54).). The '384 application issued as the '506 patent on December 15, 2009, and names Mark M. Leather and Eric Demers as the inventors. (*Id.* at (10), (45), (75).). The '506 patent claims priority to U.S. Provisional Application Serial No. 60/429,976, filed on November 27, 2002. (*Id.* at (60).). ATI Technologies ULC is the assignee of the '133 patent. (CX-0438; *see also* JX-0001 at (73).).

The '506 patent discloses graphics processing architecture that enables graphics data to be rendered to a larger size frame buffer. (Compl. at ¶ 31.). In some embodiments, the graphics

processing architecture includes multiple parallel graphics "pipelines." (*Id.*). Moreover, each pipeline can feature a special circuit that is programmable to perform texture shading in addition to color shading operations. (*Id.*). Based on the innovations disclosed by the '506 patent, modern graphics processors are able to deliver higher-quality realism of three-dimensional graphics. (*Id.*).

2. Asserted Claims of the '506 Patent

Remaining asserted claims 1-5 and 8 of the '506 patent are recited below.[18] They are product claims directed to graphic chips.

> **1.** A graphics chip comprising: a front-end in the graphics chip configured to receive one or more graphics instructions and to output a geometry; a back-end in the graphics chip configured to receive said geometry and to process said geometry into one or more final pixels to be placed in a frame buffer; wherein said back-end in the graphics chip comprises multiple parallel pipelines; wherein said geometry is determined to locate in a portion of an output screen defined by a tile; and wherein each of said parallel pipelines further comprises a unified shader that is programmable to perform both color shading and texture shading..
>
> 2. The graphics chip of claim 1 wherein each of said parallel pipelines further comprises: a FIFO unit for load balancing said each of said pipelines.
>
> 3. The graphics chip of claim 1 wherein each of said parallel pipelines further comprises: a z buffer logic unit; and a color buffer logic unit.
>
> 4. The graphics chip of claim 3 wherein said z buffer logic unit interfaces with said scan converter through a hierarchical Z interface and an early Z interface.
>
> 5. The graphics chip of claim 3 wherein said z buffer logic unit interfaces with said unified shader through a late Z interface.
>
> 8. The graphics chip of claim 1 wherein the unified shader is operative to operative to apply a programmed sequence of instructions to rasterized values and is operative to loop back to process operations for color shading

[18] Bolded patent claim numbers indicate independent claims.

and/or texture address shading.

(*Id.* at 14:30-56, 14:66–15:3.).

C. U.S. Patent No. 7,796,133 ("the '133 Patent")

1. Overview of the '133 Patent

The '133 patent, titled "Unified Shader," was filed on December 8, 2003, as U.S. Patent Application Serial No. 10/730,965 ("the '965 application"). (JX-0003 at (21), (22), (54).). The '965 application issued as the '133 patent on September 14, 2010, and like the '506 patent, names Mark M. Leather and Eric Demers as the inventors. (*Id.* at (10), (45), (75).). The '965 application is a continuation of U.S. Patent Application Serial No. 10/716,946 ("the '946 application"),[19] filed November 18, 2003, now abandoned, which claims priority to U.S. Provisional Application Serial No. 60/427,338, filed on November 18, 2002. (*Id.* at (60), (63).). ATI Technologies ULC is the assignee of the '133 patent. (CX-0440; *see also* JX-0003 at (73).).

The '133 patent relates generally to specialized texture processing circuitry that is employed by GPUs. (Compl. at ¶ 39.). As discussed in Section IV.A above, texture processing is a technology that is used, for example, to allow a 2-D image of a brick wall to be mapped to a 3-D wall object in a perspective-correct way. (*See* Figure No. 9, *supra.*).

The '133 patent provides a specialized circuit that is capable of performing both texture and color operations. (*Id.* at ¶ 41.). The claimed circuit architecture employs a combination of fixed-function and programmable circuitry stages for texture and color operations. (*Id.*). In some embodiments, any operation, be it for color shading or texture shading, may loop back and be combined with any other operation. (*Id.*). As a result, the '133 patent simplifies the

[19] The '703 application issued as the '564 patent, which Complainants terminated from this Investigation. (*See* Order No. 50 (Aug. 25, 2017).).

complexity of programming for two separate conventional fixed-function circuits with different levels of precision. (*Id.*). In addition, the '133 patent provides improved utilization of graphics circuitry, which enables system manufacturers to build more power-efficient graphics circuitry. (*Id.*).

2. Asserted Claims of the '133 Patent

Remaining asserted claims 1 and 3 of the '133 patent are recited below.[20] They are product claims directed to unified shaders.

> **1.** A unified shader comprising: an input interface for receiving a packet from a rasterizer; a shading processing mechanism configured to produce a resultant value from said packet by performing one or more shading operations, wherein said shading operations comprise both texture operations and color operations and comprising at least one ALU/memory pair operative to perform both texture operations and color operations wherein texture operations comprise at least one of: issuing a texture request to a texture unit and writing received texture values to the memory and wherein the at least one ALU is operative to read from and write to the memory to perform both texture and color operations; and an output interface configured to send said resultant value to a frame buffer.
>
> 3. The shader of claim 1 wherein said output interface sends said value to said frame buffer using a valid-ready protocol.

(JX-0003 at 11:49-64, 12:1-3.).

V. THE PRODUCTS AT ISSUE.

A. Respondents' Accused Products

The Accused Products in this Investigation incorporate [redacted]. The Accused "Singlepipe" Products ("Accused Singlepipe Products") incorporate [redacted]

[20] Bolded patent claim numbers indicate independent claims.

[redacted].[21] The Accused "Multipipe" Products ("Accused Multipipe Products") incorporate the [redacted].

Complainants' list of accused products distinguishes between the Accused Singlepipe Products and the Accused Multipipe Products. (CPBr. at App. A.). Complainants alleged that the Accused Singlepipe Products infringe claims 1 and 3 of the '133 patent, and that the Accused Multipipe Products infringe all of the asserted patent claims.

1. Respondent VIZIO's Accused Products

Chart No. 7: Accused VIZIO Singlepipe Products

Accused VIZIO Singlepipe Product	Integrated Circuit	Graphics Processor Model
[redacted]	[redacted]	[redacted]
[redacted]	[redacted]	[redacted]
[redacted]	[redacted]	[redacted]

(CPBr. at App. A.).

Chart No. 8: Accused VIZIO Multipipe Products

Accused VIZIO Multipipe Product	Integrated Circuit	Graphics Processor Model
[redacted]	[redacted]	[redacted]

[21] [redacted]. (Tr. (Reinman) at 194:11-12.).

Accused VIZIO Multipipe Product	Integrated Circuit	Graphics Processor Model
[redacted]		
[redacted]	[redacted]	
[redacted]	[redacted]	[redacted]
[redacted]	[redacted]	[redacted]
[redacted]	[redacted]	[redacted]

2. Respondent MediaTek's Accused Products

Chart No. 9: Accused MediaTek Singlepipe Product

Accused MediaTek Singlepipe Product	Graphics Processor Model

Chart No. 10: Accused MediaTek Multipipe Products

Accused MediaTek Multipipe Product	Graphics Processor Model

3. Respondent SDI's Accused Products

Chart No. 11: SDI Accused Multipipe Products

Accused SDI Multipipe Product	GPU

Accused SDI Multipipe Product	GPU

Complainants' DI Products

Complainants asserted, and Respondents did not dispute, that Complainants meet the technical prong of the domestic industry requirement. (JX-0009C (DI Stip.) at ¶¶ 2, 4, 6.). The DI Products use Complainants' GFX 8, GFX 8.1, GFX 9 GPUs. (CBr. at 10.). The DI Products consist of Complainants' "Single Shader" Products,[22] which incorporate a single shader engine, and Complainants' "Multi Shader" Products,[23] which incorporate multiple shader engines. (Tr. (Reinman) at 310:20–312:20; CX-1091C.).

[22] The following are the Single Shader Products: Bristol Ridge, Carrizo, Iceland, Stoney Ridge, and Raven Ridge.

[23] The following are the Multi Shader Products: Polaris 10, Polaris 11, Polaris 12, Polaris 22, Tonga, Vega 10, Vega 12, and Vega 20.

Set forth below are the DI Products and the claims practiced by each product.

Chart No. 12: DI Products and Claims Practiced

DI Products	'506 Patent Claims Practiced	'133 Patent Claims Practiced
Bristol Ridge	1, 8, 9	1, 3, 8, 40
Carrizo	1, 8, 9	1, 3, 8, 40
Fiji	1-9	1, 3, 8, 40
Iceland	1, 8, 9	1, 3, 8, 40
Polaris 10	1-9	1, 3, 8, 40
Polaris 11	1-9	1, 3, 8, 40
Polaris 12	1-9	1, 3, 8, 40
Polaris 22	1-9	1, 3, 8, 40
Tonga	1-9	1, 3, 8, 40
Stoney Ridge	1, 8, 9	1, 3, 8, 40
Raven Ridge	1, 8, 9	1, 3, 8, 40
Vega 10	1-9	1, 3, 8, 40
Vega 12	1-9	1, 3, 8, 40
Vega 20	1-9	1, 3, 8, 40

(JX-0009C at 2 (Table 1).).

Respondents stipulated that each of Complainants' DI Products listed in the chart above practice the corresponding patent claims from the asserted patent. (*Id.* at ¶ 4.).

VI. THE ASSERTED PATENTS

A. Level of Ordinary Skill in the Art

1. Relevant Law

The relevant time for assessing the level of ordinary skill in the art is the effective filing date of the patent. *Phillips v, AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc) ("We have made clear, moreover, that the ordinary and customary meaning of a claim term is the

meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.")

Factors to consider in determining the level of ordinary skill in the art include: (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) the prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of active workers in the field. *See Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983). "These factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art." *Daiichi Sankyo Co., Ltd. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

2. Definition of Person of Ordinary Skill in the Art

It was determined that a person of ordinary skill in the art, for the relevant timeframe of the Asserted Patents, would be one with a degree in electrical engineering, computer engineering, computer science, or a related field, and at least two (2) to four (4) years of experience working in computer graphics hardware, computer architecture, or related fields, or an equivalent combination of graduate education and/or work experience. (*Markman* Order Tr. at 11:23–12:10.).

B. Claim Construction[24]

1. Relevant Law

Claim construction begins with the plain language of the claims themselves. Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art, viewing the claim terms in the context of the entire patent. *Phillips v. AWH*

[24] The claim constructions for the agreed upon and disputed claim terms are listed in Sections VII.C and VIII.B, *infra*.

Corp., 415 F.3d 1303, 1312-13 (Fed. Cir. 2005), *cert. denied*, 546 U.S. 1170 (2006). In some cases, the plain and ordinary meaning of the claim language is readily apparent and claim construction will involve little more that "the application of the widely accepted meaning of commonly understood words." *Id.* at 1314. In other cases, claim terms have a specialized meaning and it is necessary to determine what a person of ordinary skill in the art would have understood the disputed claim language to mean by analyzing "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, as well as the meaning of technical terms, and the state of the art." *Id.* (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004)).

The claims themselves provide substantial guidance as to the meaning of disputed claim language. *Id.* "[T]he context in which a term is used in the asserted claim can be highly instructive." *Id.* Likewise, other claims of the patent at issue, "both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term." *Id.* (citation omitted).

With respect to claim preambles, a preamble may limit a claimed invention if it: (i) recites essential structure or steps; or (ii) is "necessary to give life, meaning, and vitality" to the claim. *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) (citations omitted). The Federal Circuit has explained that a "claim preamble has the import that the claim as a whole suggests for it. In other words, when the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." *Id.* (quoting *Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995)). When used in a

patent preamble, the term "comprising" is well understood to mean "including but not limited to," and thus, the claim is open-ended. *CIAS, Inc. v. Alliance Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007). The patent term "comprising" permits the inclusion of other unrecited steps, elements, or materials in addition to those elements or components specified in the claims. *Id.*

In cases where the meaning of a disputed claim term in the context of the patent's claims remains uncertain, the specification is the "single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1321. Moreover, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Id.* at 1316. As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323.

The prosecution history may also explain the meaning of claim language, although "it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1317. The prosecution history consists of the complete record of the patent examination proceedings before the U.S. Patent and Trademark Office ("PTO"), including cited prior art. *Id.* It may reveal "how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

If the intrinsic evidence is insufficient to establish the clear meaning of a claim, a court may resort to an examination of the extrinsic evidence.[25] *Zodiac Pool Care, Inc. v. Hoffinger*

[25] "In those cases where the public record unambiguously describes the scope of the patented invention,

Indus., Inc., 206 F.3d 1408, 1414 (Fed. Cir. 2000). Extrinsic evidence may shed light on the relevant art, and "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317. In evaluating expert testimony, a court should disregard any expert testimony that is conclusory or "clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent." *Id.* at 1318. Expert testimony is only of assistance if, with respect to the disputed claim language, it identifies what the accepted meaning in the field would be to one skilled in the art. *Symantec Corp. v. Comput. Assocs. Int'l, Inc.*, 522 F.3d 1279, 1289 n.3., 1290-91 (Fed. Cir. 2008). Testimony that recites how each expert would construe the term should be accorded little or no weight. *Id.* Extrinsic evidence is inherently "less reliable" than intrinsic evidence, and "is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence." *Phillips*, 415 F.3d at 1318-19.

VII. U.S. PATENT NO. 7,663,506

A. Legal Standard: Direct Infringement

"Determination of infringement is a two-step process which consists of determining the scope of the asserted claim (claim construction) and then comparing the accused product . . . to the claim as construed." *Certain Sucralose, Sweeteners Containing Sucralose, and Related Intermediate Compounds Thereof*, Inv. No. 337-TA-604, Comm'n Opinion at 36 (U.S.I.T.C., April 28, 2009) (citing *Litton Sys., Inc. v. Honeywell, Inc.*, 140 F.3d 1449, 1454 (Fed. Cir. 1998)).

---

reliance on any extrinsic evidence is improper." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

An accused device literally infringes a patent claim if it contains each limitation recited in the claim exactly. *Litton*, 140 F.3d at 1454. Each patent claim element or limitation is considered material and essential. *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538 (Fed. Cir. 1991). In a Section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a preponderance of the evidence. *Enercon GmbH v. Int'l Trade Comm'n,* 151 F.3d 1376, 1384 (Fed. Cir. 1998). If any claim limitation is absent, there is no literal infringement of that claim as a matter of law. *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000).

B. Infringement Overview

Complainants alleged that the Accused Multipipe Products infringe claims 1-5 and 8 of the '506 patent ("the '506 Accused Multipipe Products"). (CPBr. at 18-26; CBr. at 26-66.). Complainants and Respondents stipulated that the following are representative of the Accused Multipipe Products that Complainants have accused of infringing the asserted claims of the '506 patent.

Chart No. 13: Accused Multipipe Products

Accused VIZIO Products covered by Representative Product	VIZIO Rep. Product	System Prod. Category	Commercial Name	Graphics Processor Model Name
All accused VIZIO products that contain a				
All accused VIZIO products that contain a				
All accused VIZIO				

Accused VIZIO Products covered by Representative Product	VIZIO Rep. Product	System Prod. Category	Commercial Name	Graphics Processor Model Name
products that contain an				

(JX-0011C (Representative Prods. Stip.) at 2-4.).

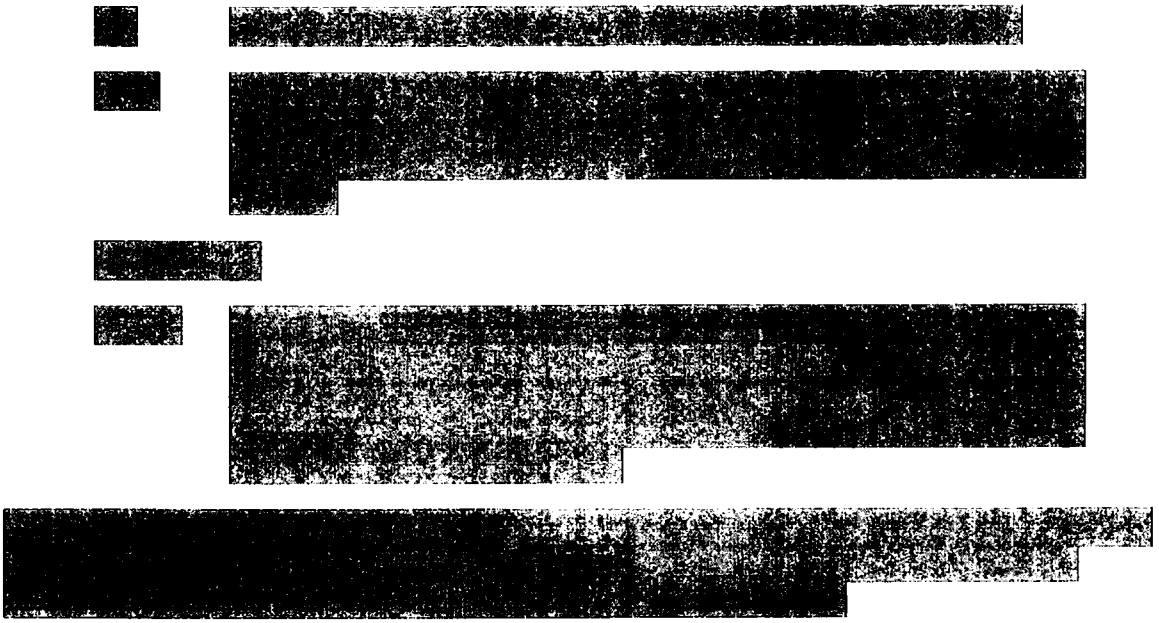
Complainants and Respondents stipulated that each of the '506 Accused Multipipe Products incorporates an SoC with either an . (*Id.*; *see also* Tr. (Reinman) at 192:15-24.). For infringement analysis purposes, the . (Tr. (Reinman) at 194:7-12.).

There is no dispute that the structure, function, and operation of the in the '506 Accused Multipipe Accused Products are defined by . (Tr. (Reinman) at Tr. 195:9–196:5;

Tr. (Larri) at Tr. 518:5-17.). Respondents' fact witness, Mr. Larri, described the [redacted]. (Tr. (Larri) at 686:1-20.). In addition, Mr. Larri testified that [redacted]. (Tr. (Larri) at 685:22–686:5.). Mr. Larri and Dr. Reinman, Complainants' expert, agreed that [redacted]. (Tr. (Reinman) at 220:15-24; Tr. (Larri) at 686:1-20.).

[redacted]

* * *



There is no evidence offered in this Investigation indicating that Respondents MediaTek or SDI have [redacted]. This issue was never raised.

Thus, there is no dispute that the [redacted] accurately describes the structure, function, and operation of the '506 Accused Multipipe Products. (*See, e.g.*, CX-0263SC (Dep. Tr. of Jacques Martinella[26] (June 30, 2017)) at 21:5-22:17 ([redacted]).).

Based on the [redacted], and evidence presented in this Investigation, the '506 Accused Multipipe Products infringe the asserted claims of the '506 patent.

[26] When he testified during his deposition on June 30, 2017, Mr. Jacques Martinella was the Vice President of Hardware Engineering at Sigma Designs. (CX-0263SC at 8:24–9:1.). SDI identified Mr. Martinella as a 30(b)(6) witness to testify on certain topics on behalf of SDI.

C. Relevant Claim Terms

The following constructions of the claim terms recited in the asserted claims of the '506 patent have been agreed upon by the parties or adopted by this Court.[27]

Chart No. 14: Constructions of Claim Terms Relevant to the '506 Patent

Claim Term	Construction
"front-end in the graphics chip" (claim 1)	Plain meaning, such as section of graphics chip that receives graphics instructions as input and generates geometry as output. (*Markman* Order Tr. at 16:10-16.).
"back-end in the graphics chip" (claim 1)	Section of graphics chip that processes geometry received as input. (*Id.* at 16:17-25.).
"frame buffer" (claim 1)	Plain meaning, such as memory that maps an image from a complete frame of pixels to a display. (*Id.* at 17:2-11.).
"unified shader" (claims 1, 5, and 8)	A single shader circuit capable of performing color shading and texture coordinate shading. (*Id.* at 13:10-24.).
"texture shading" (claims 1 and 8)	Plain meaning, texture shading operations including coordinate texture mapping and texture address operations. (*Id.* at 17:14–18:9.).
"determined to locate in a portion of an output screen defined by a tile" (claim 1)	Determined to correspond to a portion of an output screen defined by a tile. (*Id.* at 18:10-22.).
"operative to operative" (claim 8)	Operative, obvious typographical error. (*Id.* at 20:18–21:2.).

[27] The Parties disputed the meaning of additional claim terms recited in claims that have been terminated from this Investigation. Those terms are not included in Chart No. 14.

D. The'506 Accused Multipipe Products Infringe Claims 1-5 and 8 of the '506 Patent

1. Claim 1 of the '506 Patent

a) "A graphics chip comprising"

Evidence presented in this Investigation demonstrates that each of the '506 Accused Multipipe Products includes an , which is a graphics chip as recited in the preamble. (CX-3752C (VIZIO Resp. to Interrog. No. 2) at 57-71; CX-3848C (MediaTek Resp. to Interrog. No. 2) at 12-14; CX-3872C (SDI Resp. to Interrog. Nos. 1-2) at 11-13; Tr. (Reinman) 238:18–240:5, 246:2-9; CX-1435C ( )[28] at 15 (emphasis in the original)), 20; CX-2228C ( ) at 6 (emphasis in the original)); *see also* CDX-0100.48.).

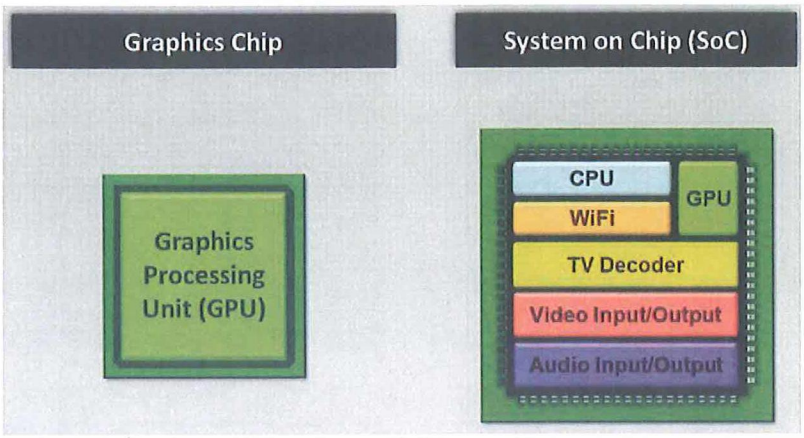
Respondents' non-infringement expert, Dr. Lastra, did not dispute that each of the '506 Accused Multipipe Products contains an integrated circuit that . (Tr. (Lastra) at 727:17-23.). He also agreed that "GPUs like the perform graphics processing." (*Id.* at 792:7-12.). Rather, Dr. Lastra opined that an integrated chip that ***only*** performs graphics processing is a graphics chip. (*Id.* at 745:12–746:19; RPBr. at 12-13; RRBr. at 8-13.). According to Dr. Lastra's definition, regardless of whether an integrated circuit performs graphics processing, it would not qualify as a graphics chip if it contains additional circuitry for, among other things, watching TV or a DVD, video processing, or MPEG decoding.[29] (Tr. (Lastra) at 746:5-19, 794:19–797:3, 798:17–800:6.). Referring, *inter alia*, to

[28] . (Tr. (Reinman) at 284:25–285:1.).

[29] The meaning of "graphics chip" was not disputed during the claim construction proceedings in this

Figure No. 10 below, Dr. Lastra provided the following testimony in which he distinguished a "graphics chip" from an SoC.

Figure No. 10: Demonstrative Exhibit Comparing a Graphics Chip with a SoC



(RDX-0002C.0017.).

> Q: Would one of ordinary skill in 2002 consider an SOC and a graphics chip the same thing in your opinion?
>
> A: No, not at all.

Investigation. (*See* Doc. ID No. 628332 (Revised Joint Claim Construction Chart) (Nov. 7, 2017).). Thus, "graphics chip" is construed consistent with its plain meaning to one of ordinary skill in the art. During *Markman* briefing, in the context of the Parties' proposed constructions of a "unified shader," there was some dispute with respect to whether Respondents' proposal of a "single graphics processor ***component***" is hardware or software. (Comp'ls Claim Br. at 33-34 ("[I]n all claimed embodiments, the unified shader is 'programmable.' [I]t would belie common sense how a component, such as software, could in and of itself, be programmable. . . . Both the '506 and '133 Patents are in the field of 'computer graphics chips,' which is hardware."); *Markman* Hearing Tr. at 11:12–12:23("Let's go back to what [Complainants] say. 'Both the '506 and '133 patents are in the field of computer graphics chips, which is hardware.' We agree. Components are chips. The patents say so."). The Parties agreed during the *Markman* Hearing that "component" is hardware. (*Markman* Hearing Tr. at 23:5–24:4 ("[I]t wasn't clear from the briefing . . . whether Respondents were conceding that the unified shader had to be hardware. So there is no dispute on our end. It has to be hardware. We thought the component would actually include the possibility of software, and it wasn't clear from the briefing, in our mind, whether Respondents were conceding that point. So we have no objection to the concept that the component, to the extent the Court adopts that, must be circuitry, it has to be hardware, and it can't be software. So we don't disagree in that regard.").).

> Q: Why not?
>
> A: They're not the same. The one on the left is a chip that just has a graphics core or a GPU, your Honor. And the one on the right, and the way my slides were set up, you could see -- there we go. They have all sorts of stuff. In fact, in this investigation, those chips would have a lot of circuitry for TVs, because that's what they do, they run TVs. This particular illustration is also showing Wi-Fi, so it would have radios for Wi-Fi, a CPU to run the whole thing, and then a GPU in the corner.

(Tr. (Lastra) at 746:5-19.).

Dr. Lastra's testimony is contradicted by the intrinsic evidence. For example, the file history of the '506 patent explicitly states that, "[a]s to claims 1, 9, and 17 . . . the claims are directed to a graphics chip, such as an integrated circuit that ***at least*** performs graphics processing." (JX-0002.0084 (emphasis added), 0077; *see also* Tr. (Reinman) at 238:18-24.). Additionally, in considering this definition during cross-examination, Dr.Lastra opined that if "graphics chip" is construed as "an integrated circuit that at least performs graphics processing, then the [accused] SOCs are . . . graphics chips." (Tr. (Lastra) at 807:12-20; *see also id.* at 807:21–808:10.).

Moreover, and as Staff agreed, the language of the preamble uses the open-ended term "comprising" to denote that a graphics chip must include, but is not necessarily limited to, circuitry for performing graphics processing. (JX-0001 at 14:30.). The use of the open-ended term "comprising" means that the graphics chip is presumed to encompass all of the graphics processing elements recited in the claim, but can also include additional, unrecited non-graphics elements. *See, e.g., Crystal Semiconductor Corp. v. TriTech Microelectronics Int'l Inc.*, 246 F.3d 1336, 1348 (Fed. Cir. 2001) ("[T]he transition 'comprising' creates a presumption that the recited elements are only a part of the device, that the claim does not exclude additional, unrecited elements.").

For the reasons discussed above, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet the preamble recited in claim 1.

b) "a front-end in the graphics chip configured to receive one or more graphics instructions and to output a geometry"

The record evidence establishes that each of the '506 Accused Multipipe Products contains a front-end in the graphics chip configured to receive one or more graphics instructions and to output a geometry. (Tr. (Reinman) at 246:10–249:25.). A "front-end in the graphics chip" was given its plain meaning, such as a section of a graphics chip that "receives graphics instructions as input and generates geometry as output." (*Markman* Order Tr. at 16:10-16.).

Based on relevant technical documents and source code, Dr. Reinman opined that each [redacted] includes a geometry processor ([redacted])[30] at a front-end. (Tr. (Reinman) at 247:1-13; CDX-0006C; CX-1435C.0025.).[31]

Dr. Reinman testified that the geometry processor includes **a** [redacted] (Tr. (Reinman) at 247:20–248:9; CDX-0006C; CX-1435C.0025.). The [redacted] receives graphics instructions, in the form of [redacted], along with other signals, over the [redacted],[32] [redacted]

[30] [redacted]. (Tr. (Reinman) at 247:14-19.).

[31] CDX-0006C is a demonstrative exhibit that Dr. Reinman created [redacted]. (Tr. (Reinman) at 218:13–219:10, 228:11-19, 229:18–230:8.).

[32] Dr. Reinman described the [redacted] (Tr. (Reinman) at 249:6-10.).

[redacted].[33] (Tr. (Reinman) at 247:20–248:9; CDX-0006C; CX-1435C.0025.).

The [redacted]. (Tr. (Reinman) at 166:12-25, 248:14–249:5; CDX-0006C; CX-1435C.0035-36.).

Respondents argued that the [redacted] does not ***receive*** graphics instructions. (RPBr. at 14; RRBr. at 13-14.). Respondents relied on Dr. Lastra's opinion that commands [redacted] are not "instructions." (Tr. (Lastra) at 755:12–756:19.). However, as Complainants noted, there is no disavowal in the '506 patent that warrants Dr. Lastra's interpretation of the term "instructions" to exclude such commands. *See, e.g.*, *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed. Cir. 2004) ("Absent a clear disavowal or contrary definition in the specification or the prosecution history, the patentee is entitled to the full scope of its claim language."). Additionally, Dr. Lastra did not dispute that the [redacted] and failed to offer a plausible explanation why these [redacted] are not instructions. (Tr. (Lastra) at 755:12–756:19.).

---

[33] To the extent that a definition of a [redacted] was proffered, Mr. Larri provided the following description: [redacted] (Tr. (Larri) at 617:13-24.).

[34] [redacted] is an acronym for [redacted] (Tr. (Reinman) at 248:18-20.).

Dr. Lastra also failed to address Dr. Reinman's opinion and analysis that, separate and independent of the [redacted], "instructions" are also brought into the [redacted] by the [redacted], which is evidenced by [redacted] (emphasis added); CX-1435C.0033 [redacted]. Moreover, Dr. Lastra's unsupported opinion contradicts [redacted] technical documents and source code. (CX-1435C.0246 ([redacted]); CX-1435C.0251 ([redacted]).

With regard to the "output a geometry" limitation, ARM's fact witness, Mr. Larri, contended that the [redacted] in the '506 Accused Multipipe Products only "[redacted]," and does not "[redacted] any geometry." (Tr. (Larri) at 597:12-19 [redacted].). Mr. Larri's testimony fails on a number of grounds.

First, [redacted] technical documents and source code indicate that [redacted] (CX-1435C.0029.). Dr. Reinman based

his opinion that the [redacted] identified by Mr. Larri. (Tr. (Reinman) at 248:18-24 [redacted]

Second, as Complainants pointed out, Mr. Larri's testimony contradicts statements Respondents made in their initial claim construction brief. For instance, Respondents equated vertex transformation [redacted]. (Resp'ts Claim Br. at 33 ("As these chapters in the Foley reference teach (consistently with the teaching of the '506 patent), 'the output of the front-end subsystem is typically a set of primitives in screen coordinates ***generated through vertex transformation***.'") (emphasis added); *id.* at 34 ("Thus, the front-end in the graphics chip is responsible for generating geometry based on graphics instructions, ***which the specification unambiguously explains is done by performing vertex transformation***.") (emphasis added).). Thus, Mr. Larri's testimony has been given limited weight.

Finally, during the *Markman* hearing, Respondents argued that the front-end could also contain primitive assembly circuitry for generating geometry as output.

> The graphics assembly is not the back end. It's not. How do we know that? Let's go on to the next slide. What we see is that the graphics assembly is the thing that's sending these primitives, the geometry. That's the thing that's sending the geometry on. And what do we know about the geometry? Where is the geometry coming from? The front end. We know that. We know that from the claim, and we actually know that from the constructions that are being offered by the Complainant and the Staff. ***We know that the front end generates geometry as output. What is generating the geometry as output? It's a part of that 510, that graphics assembly as shown here in the figure 5***. So that's not the

back end.

(*Markman* Hearing Tr. at 69:8-20 (emphasis added).).

Accordingly, for the foregoing reasons, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this limitation of claim 1.

c) "a back-end in the graphics chip configured to receive said geometry and to process said geometry into one or more final pixels to be placed in a frame buffer"

Evidence proffered in this Investigation demonstrates that each of the '506 Accused Multipipe Products contains a back-end in the graphics chip configured to receive said geometry and to process said geometry into one or more final pixels to be placed in a frame buffer. (Tr. (Reinman) at 250:1–254:7.). A "back-end in the graphics chip" was construed to mean a section of a graphic chip that "processes geometry as input." (*Markman* Order Tr. at 16:17-25.).

In particular, the record evidence reflects that each used in the '506 Accused Multipipe Products includes a back-end comprising either . (Tr. (Reinman) at 250:20–251:2; CDX-0006C; CX-1435C.0023; JX-0011C.0002-3.). As Dr. Reinman opined,

. (Tr. (Reinman) at 251:3-13; CDX-0006C.).

Based on source code and technical documents provided by Dr. Reinman testified that the into final pixels by . (Tr. (Reinman) at 251:14–253:6; CDX-0006C; CX-1435C.0029-30, 36-38.). Dr. Reinman also testified that the '506 Accused MediaTek and SDI Multipipe Products are configured to process

geometry into final pixels that are to be placed in a frame buffer that maps an image from a complete frame of pixels in a display. (Tr. (Reinman) at 253:7–254:7; CX-1435C.0030; CX-1490C.0021, 27-28; CDX-0006C.). Additionally, Dr. Reinman opined that the '506 Accused VIZIO Multipipe Products actually place the final pixels, [redacted], into the VIZIO television's system [redacted], which maps an image from a complete frame of pixels to the VIZIO television display. (Tr. (Reinman) at 1310:20–1311:20; CX-2724.0009.).

Respondents asserted that the alleged "back-end" of the SoCs containing an [redacted] does not produce "one or more ***final*** pixels" and does not place these produced pixels in a "frame buffer" on the SoCs.[35] (RRBr. at 14-19 (emphasis in original).). Neither assertion is supported by the evidence.

With regard to Respondents' "final pixels" argument, [redacted] technical documents specify that: (1) [redacted] (CX-1490C.0021 (emphasis added)); (2) the [redacted] (*id.* at 1490C.0024 (emphasis added); and (3) [redacted] (*id.* at 1490C.0027 (emphasis added).). The technical documents also disclose that [redacted] (*Id.* at 1490C.0028 (emphasis added).).

With respect to Respondents' "frame buffer" contention, this limitation merely requires

[35] "[F]rame buffer" was construed to mean a "memory that maps an image from a complete frame of pixels to a display." (*Markman* Order Tr. at 17:2-11.).

that "a back-end in the graphics chip [be] configured to receive said geometry and to process said geometry into one or more final pixels ***to be placed*** in a frame buffer." (JX-0001.0025 at 14:33-35 (emphasis added).). In other words, the accused product need only contain a "back-end in the graphics chip" structure that is capable of performing the recited function "configured to receive said geometry and to process said geometry into one or more final pixels to be placed in a frame buffer." *UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816, 827 (Fed. Cir. 2016) (holding that "the 'data generating' limitations only indicate that the associated structures have this capability . . . and do not require that any data be actually generated by the user"). Thus, that the SoCs in the '506 Accused MediaTek and SDI Multipipe Products do not [redacted] has no bearing on whether these products meet this limitation.

During the *Markman* proceedings in this Investigation, Respondents proposed that a "frame buffer" be construed to mean a "back-end component to store a complete frame of final pixels." (*See* Res'pts Claim Br. at 38.). Respondents' proposed construction was rejected. The adopted construction did not include any limitations on where the claimed frame buffer must be located. Respondents' inappropriate attempt to re-argue the construction of a "frame buffer" thus fails.

Moreover, based on his review of the technical documents and source code, Dr. Reinman's opinion that the '506 Accused VIZIO Mutipipe Products contain a frame buffer, is effectively unrebutted. (Tr. (Reinaman) at 253:7–254:2, 1310:20–1311:20; Tr. (Lastra) at 756:20–761:2.). When pressed on cross-examination as to whether the'506 Accused VIZIO Multipipe Products could even work without a frame buffer, Dr. Lastra responded that he could not "say that for sure" because he did not know "whether there's something ***unusual*** in the VIZIO TVs." (Tr. (Lastra) at 843:11–844:2 (emphasis added); *cf.* Tr. (Reinman) at 1311:12-20

(Dr. Reinman confirming that a VIZIO TV would not work without a frame buffer because "[t]he expectation is that there would be some form of buffering for an entire frame to be drawn out so that it's ready for display."). In other words, the ***usual*** circuitry would include a frame buffer. Accordingly, Dr. Lastra's opinion is given little to no weight.

Thus, for the reasons discussed above, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this limitation of claim 1.

d) "wherein said back-end in the graphics chip comprises multiple parallel pipelines"

The evidence adduced in this Investigation establishes that the back-end of the in each of the '506 Accused Multipipe Products comprises multiple parallel pipelines. (Tr. (Reinman) at 254:8–255:3.). The in each '506 Accused Multipipe Product includes either , each of which serves as one of the multiple parallel pipelines. (*Id.*; CDX-0006C; CX-1435C.0023; JX-0011C.0002-3.). Respondents offered no rebuttal to this evidence.

For these reasons, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this limitation of claim 1.

e) "wherein said geometry is determined to locate in a portion of an output screen defined by a tile"

The record evidence reflects that the geometry output by the front-end of the in each of the '506 Accused Multipipe Products is determined to locate in a portion of an output screen defined by a tile.[36] (Tr. (Reinman) at 255:4–258:9.). As discussed in Section VII.D.1(a)

[36] Dr. Reinman describes a tile as follows: "[Y]ou could think of a tile as being a rectangular grid that could be overlaid on top of a display screen. So each one of those tiles is a particular piece of the display screen. And we're going to work on one part of that in the tile buffer and then offput it -- output it to the frame buffer. And so the frame buffer will hold the entirety of the frame all the times [sic], but we will

above with regard to the preamble of claim 1, the [redacted] (front-end of the graphics chip) includes a [redacted]. (*Id.* at 248:14-24, 255:21-256:6; CDX-0006C; CX-1435C.0029.). The [redacted] (*Id.* at 255:21–257:23; CDX-0006C.). [redacted] (*Id.* at 257:15–258:4.). Respondents offered no non-infringement position on this claim element during the evidentiary hearing. (Tr. (Lastra) at 761:22–762:5; *see also* RRBr. at 19-20.).

Accordingly, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this limitation of claim 1. Moreover, Respondents have waived any arguments under Ground Rule 10.1.

f) "wherein each of said parallel pipelines further comprises a unified shader that is programmable to perform both color shading and texture shading"

Evidence submitted in this Investigation demonstrates that each of the '506 Accused Multipipe Products contains parallel pipelines further comprising a unified shader that is programmable to perform both color shading and texture shading. (Tr. (Reinman) at 258:11–265:14.).

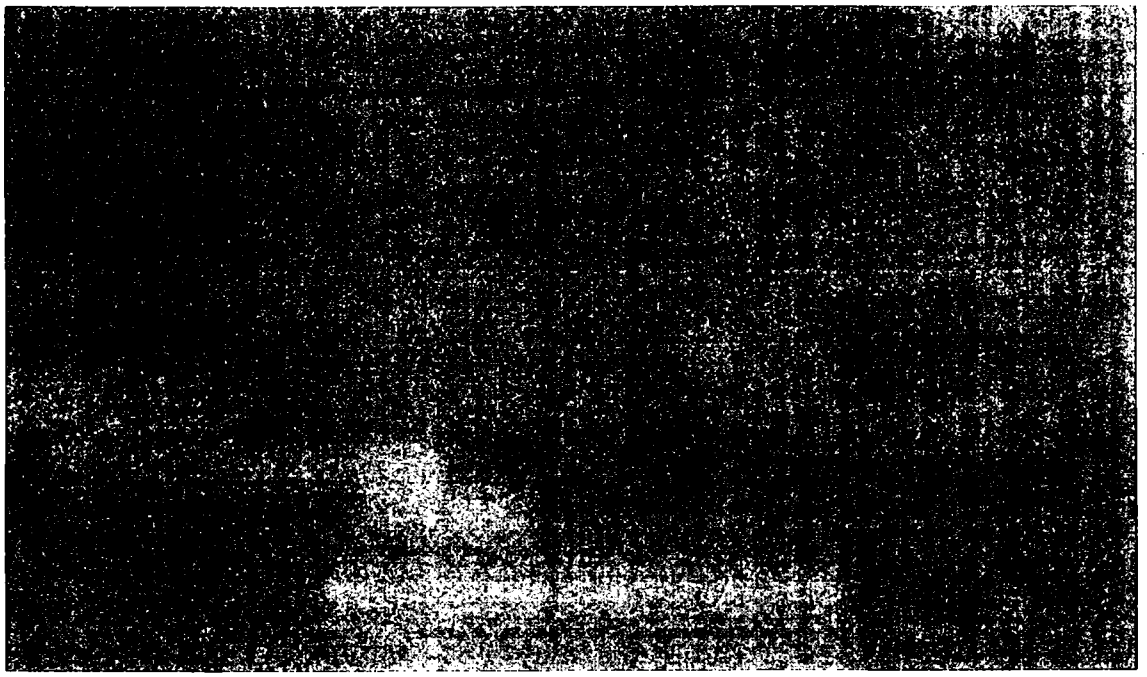
A "unified shader" was construed to mean a "single shader circuit capable of performing

---

have it at a tile granularity. Locating a geometry in a tile is that useful part we talked about where the parallel pipelines can work independently because they will know what goes in a tile and the tiles will be separate." (Tr. (Reinman) at 256:14-25.).

color shading and texture coordinate shading." (*Markman* Order Tr. at 13:10-24.). The record evidence reflects that each [redacted] includes (highlighted in yellow below): [redacted] (collectively, the "[redacted]" (in blue below)). (*Id.* at 260:20–261:21.).

Figure No. 11: Dr. Reinman's Source Code Diagram Illustrating the [redacted]



(CDX-0006C (annotated).).

Dr. Reinman's testimony, and [redacted] technical documents and source code, confirm that the [redacted] uses the [redacted] (Tr. (Reinman) at 261:22–262:7; CDX-0006C;

CX-1435C.0036-38.). Dr. Reinman's testimony and the evidence he presented demonstrating that the is capable of performing ***color*** shading is unrebutted. (Tr. (Lastra) at 832:9 ("Well, I'm not disputing color shading at all.").). On cross-examination, Dr. Lastra agreed that (*Id.* at 833:16-21, 832:9.).

Respondents' non-infringement arguments focused on whether the is the claimed "unified shader," and whether the is "a single shader circuit that is capable of performing . . . texture coordinate shading," as "unified shader" been construed. (RRBr. at 20-34.).

Respondents argued that Complainants' expert, Dr. Reinman, "self-selected a subset of functional units" within the "by drawing a 'blue polygon' on the summary diagram he prepared for this investigation." (*Id.* at 20.). Respondents' expert, Dr. Lastra, testified that Dr. Reinman's blue polygon is not a single shader circuit because it contains only "bits and pieces" of the , and does not include the . (Tr. (Lastra) at 730:20–731:11.).

> A: So what Dr. Reinman has chosen is a collection of pieces of the . He hasn't taken the whole of the , right, which would be a -- certainly a . He's taken bits and pieces. So it's like taking a car, pulling off a door, pulling off the hood, a tire and saying -- putting them down on the ground, saying "that's a car."
>
> Q: Dr. Lastra, are you aware why Dr. Reinman identified certain functional blocks and excluded other in his identification of unified shader?
>
> A: Yes. My opinion is he had to exclude some blocks because other claim terms required them to be separate.

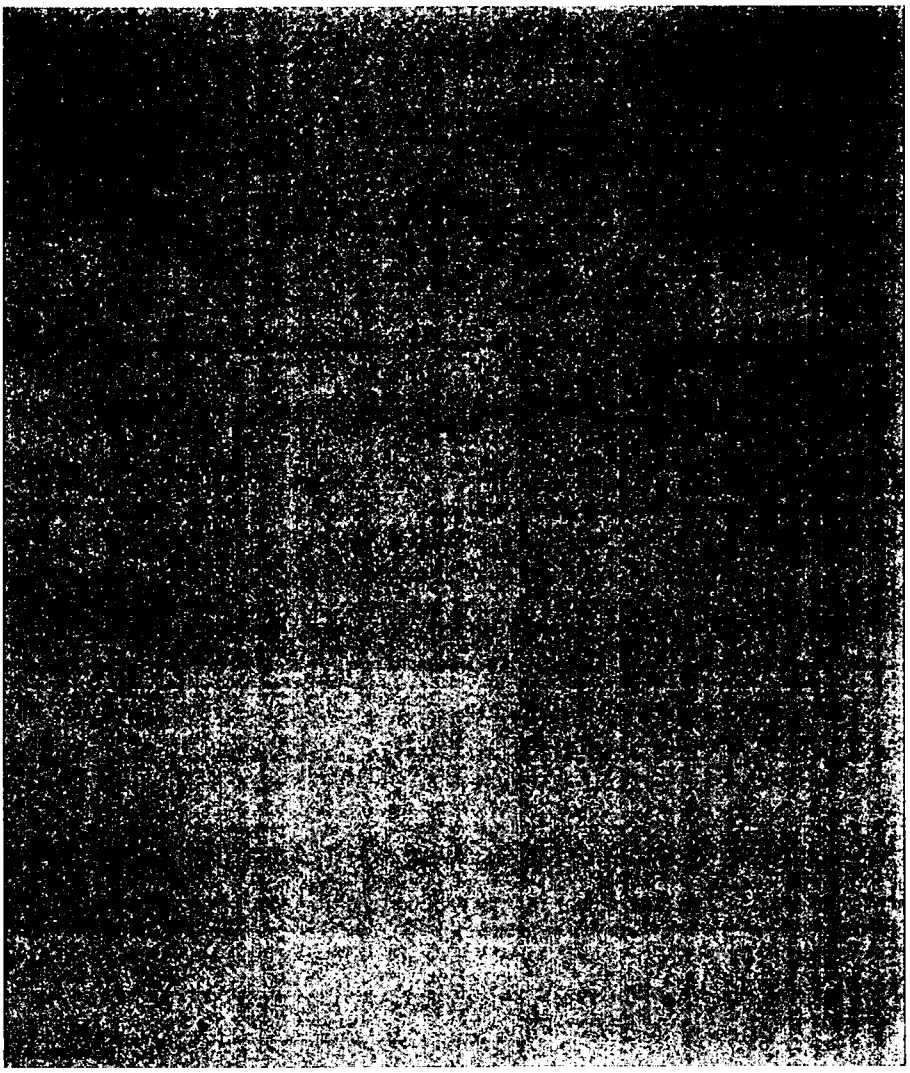
(*Id.*).

However, as Complainants noted, it is not necessary for the claimed unified shader to

read on the entirety of the [redacted] in order for the '506 Accused Multipipe Products to infringe. *Suntiger, Inc. v. Sci. Research Funding Grp.*, 189 F.3d 1327, 1336 (Fed. Cir. 1999) ("If a claim reads merely on a part of an accused device, that is enough for infringement."). As the Federal Circuit has explained, "[i]t is fundamental that one cannot avoid infringement merely by adding elements if each element recited in the claims is found in the accused device." *Stiftung v. Renishaw PLC*, 945 F.2d 1173, 1178 (Fed. Cir. 1991). For example, "a pencil structurally infringing a patent claim would not become non-infringing when incorporated into a complex machine that limits or controls what the pencil can write." *Id.* It is sufficient for the purpose of infringement that the claimed structure and function of the unified shader exists within the [redacted] of the '506 Accused Multipipe Products. *Id.* That Dr. Reinman did not identify the entirety of the [redacted] as the alleged unified shader has no bearing on whether or not the portion of the [redacted] that he did identify—the "[redacted]"—satisfies the claim limitations. *Id.*

With regard to the "single shader circuit" aspect of the construction of "unified shader," Mr. Larri, Respondents' fact witness, testified that the [redacted]. (Tr. (Larri) at 501:12-24.). Referring to Figure 2-7 (Figure No. 12) from the [redacted], below, Mr. Larri provided the following testimony:

Figure No. 12: Figure 2-7 from



(CX-1435C.0037 (Fig. 2-7).).

* * *

(Tr. (Larri) at 501:14–503:4.).

Referring to the same figure (Figure No. 12), Dr. Lastra additionally opined that Dr. Reinman's is not "unified" because the shown in Figure 2-7 (Figure No. 12) (Tr. (Lastra) at 734:13-20.).

Based on Mr. Larri's and Dr. Lastra's testimony, and, *inter alia*, Figure 2-7 (Figure No. 12), Respondents asserted that the word "circuit" in the construction of a "unified shader" does not "grant[] [Complainants] license to select (and continuously re-select) ***any*** collection of electrically-connected elements." (RRBr. at 24 (emphasis in original) (citing CBr. at 45).). However, as Complainants pointed out, Respondents' assertion is an improper attempt to re-argue the construction of this claim term. (CBr. at 45.).

During the *Markman* proceedings in this Investigation, Respondents argued that the meaning of a "unified shader" should be limited to a single "***component***," in contrast to Complainants' and Staff's proposed construction of a "single shader ***circuit***," which Respondents described as "simply a closed loop that carries electronic signals" and, thus, too broad. (Resp'ts Claim Br. at 16 (citing RXM-0012 (Newton's Telecom Dictionary (1999) (Circuit: "channels,

conductors and equipment between two given points through which an electric current may be established . . . [a] circuit can also be a network of circuit elements . . . that performs a specific function.")); *Markman* Hearing Tr. at 8:23–11:20 ("So what's the issue here? Well, it's the term 'circuit.' It's a very broad term. It's almost unbounded. In fact, Dr. Wolfe said, I think, a GPU is a circuit. A graphics processor unit is a circuit. And he's not wrong. A circuit is simply a path for electrical current. But the problem is, we have to have a single something."). In adopting Complainants' and Staff's proposed construction, Respondents' proposed construction was squarely rejected. (*Markman* Order Tr. at 13:10-24.).

Therefore, under the adopted construction of the claimed "unified shader," multiple components or units can perform color and texture operations, as long as these components or units are within the same electronic loop. The identified by Dr. Reinman thus corresponds to the claimed "unified shader."

With regard to the "texture coordinate shading" aspect of the construction of "unified shader," experts for both Complainants and Respondents agreed that texture coordinate shading is a more complex texture shading operation than texture mapping, which involves modifying texture coordinates once they are generated. (Tr. (Reinman) at 172:8–173:11, 444:11-20; CDX-0100C.0015; Tr. (Wolfe) at 1372:15–1373:3, 1377:14–1378:7.).

This is consistent with the disclosure in the '506 patent.

> A unified shader 570 works in conjunction with the texture unit 585 and applies a programmed sequence of instructions to the rasterized values. These instructions may involve simple mathematical functions (add, multiply, etc.) and may also involve requests to the texture unit. A unified shader reads in rasterized texture addresses and colors, and applies a programmed sequence of instructions. A unified shader is so named because the functions of a traditional color shader and a traditional texture address shader are combined into a single, unified shader.

(JX-0001.002 at 6:43-52.).

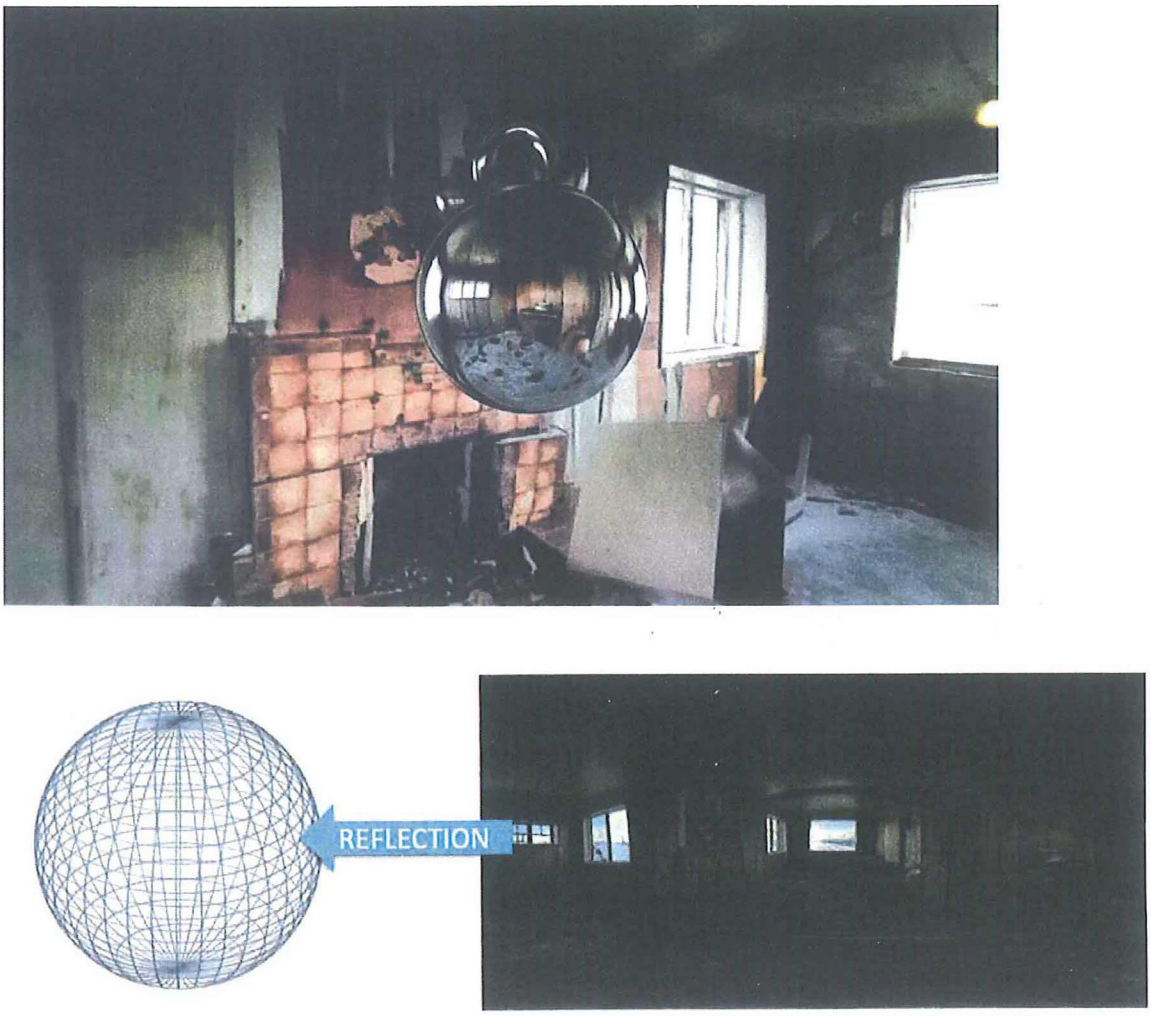
The [redacted] contains a [redacted]. (CX-1435C.0038; Tr. (Reinman) at 234:7-9, 283:6-15, 772:4-8.). The [redacted] receives those [redacted]. (CX-1435C.0037-38; CDX-0006C.). The [redacted]. (Tr. (Reinman) at 262:8-25; CDX-0006C; CX-1435C.0036-8.).

Respondents contended that the [redacted] identified by Dr. Reinman cannot meet this limitation because it excludes the [redacted]. (RRBr. at 26-27 (citing Tr. (Lastra) at 735:6–743:9; CX-1435C.0038).). Relying on testimony provided by Mr. Larri and Dr. Lastra, as well as the [redacted] Respondents argued that the [redacted] (RRBr. at 27 (citing Tr. (Larri) at 504:19–506:17; Tr. (Lastra) 736:21–737:16); *see also* CX-1435C.0038.).

There is no dispute that the [redacted]. (*See, e.g.*, CBr. at 47.). That the [redacted] (CX-1435C.0038 (emphasis added); *see also* CX-1435C.0224) does not mean that the [redacted] does not perform any texturing operations. Evidence presented in this Investigation reflects the contrary. Dr. Reinman tested one of Respondent VIZIO's accused

products, the [redacted], and confirmed that the [redacted] performs texture coordinate shading (e.g., instructions to create the reflection on a mirrored sphere (CX-1384)). (Tr. (Reinman) at 264:7–265:5 (referring to CDX-0100.69, Dr. Reinman testified that "you can see texture coordinate shading . . . in this particular code"); CDX-0100.68; CX-1384.).

Figure No. 13: Example of Texture Coordinate Shading



(CDX-0100C.0019; CDX-0100C.0069.).

Dr. Reinman's testimony, and the supporting evidence on which Dr. Reinman relied (i.e., CX-1384), was not persuasively rebutted by Respondents' expert, Dr. Lastra, who provided the

following testimony with respect to the source code contained in CX-1384:

> Q: You would agree with me that that program also modifies existing texture coordinates associated with a pixel; correct? And let's pull up slide CDX-0100.68, which is AMD 1044-0283759, and also CX-1384. So I'll ask the question again. You'll agree with me that the program shown also modifies existing texture coordinates associated with a pixel; correct?
>
> A: Give me a minute to read it. This particular slide?
>
> Q: Sorry. Next slide, please.
>
> A: Okay. ***There's one texture lookup, that's the very last thing. It's getting a color. And there's a reflection vector. So yes, it's modifying the reflection vector by multiplying it by 5 and adding -- by .5 and adding .5.***
>
> * * *
>
> Q: . . . You'll agree with me that reflectView.xy is a texture coordinate; correct?
>
> A: That's a coordinate. I don't know that it's a texture coordinate. It's used in a texture lookup and it's an environment map texture lookup.
>
> Q: You don't have enough information to know one way or another, Doctor, whether that's a texture coordinate, do you?
>
> A: And certainly not because, you know, texture coordinate is a patent term. So I would have to look some more to see whether that's actually a texture coordinate, sir.
>
> Q: ***If it was a texture coordinate, you'd agree with me that this code would be showing operations such as multiplication and division that would be modifying a texture coordinate; correct***?
>
> A: ***It's doing arithmetic, yes***.

(Tr. (Lastra) at 840:8–841:17 (emphases added).).

> Q: Yeah, my question was would the multiplication and addition that is shown in the line of code be on -- shown in that line of code that we've been talking about regarding the Reinman test, ***would that be performed inside the blue box*** that is shown on CDX-0006C?
>
> A: Well, the [redacted]. We just discussed that, whether what's in there is enough to do that arithmetic. I'd be concerned that since the [redacted] isn't in there, it might not be. I'd have to look at the code in order to tell.

(*Id.* at 842:14-23 (emphases added).).

Dr. Reinman's testimony is also consistent with the specification of the '506 patent, which discloses that the ***rasterizer***, not the unified shader, produces the texture coordinates, and that the ***unified shader*** applies texturing instructions to the rasterized texture coordinates.

> Rasterizer 560 computes up to multiple sets of 2D or 3D perspective correct texture addresses and colors for each quad.
>
> * * *
>
> A unified shader 570 works in conjunction with the texture unit 585 and applies a programmed sequence of instructions to the rasterized values. These instructions may involve simple mathematical functions (add, multiply, etc.) and may also involve requests to the texture unit. A unified shader reads in rasterized texture addresses and colors, and applies a programmed sequence of instructions.

(JX-0001 at 6:38-40, 6:43-49.).

Texture coordinate shading, as understood by those of ordinary skill in the art, supports Complainants' experts' view that such operations do not include the generation of texture coordinates, but rather, involves modifying texture coordinates ***after*** the texture coordinates are generated. (*See, e.g.*, Tr. (Wolfe) at 1377:15–1378:7 (defining texture coordinate shading and providing examples of effects achieved with texture coordinate shading); Tr. (Reinman) at 172:11–173:11, 444:11-20.).

Thus, Respondents' and Dr. Lastra's assertions that "texture coordinate shading requires operating on ***and producing*** texture coordinates" import a limitation that is not only ***not*** required by the language of claim 1 and the constructions of a "unified shader" and "texture shading," but is also ***contradicted*** by the specification of the '506 patent and how the term texture coordinate shading is used by those of ordinary skill in the art. (RRBr. at 28 (emphases added) (citing Tr. (Lastra) at 737:9-13).).

For the foregoing reasons, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this claim limitation and infringe claim 1 of the '506 patent.

2. Claim 2 of the '506 Patent

a) "The graphics chip of claim 1 wherein each of said parallel pipelines further comprises: a FIFO[37] unit for load balancing said each of said pipelines."

The evidence adduced in this Investigation establishes that the '506 Accused Multipipe Products include a FIFO that buffers and balances the workload between the front-end and back-end of the graphics chip. (*See, e.g.*, CX-1435 ( ); CX-2229C ( ).). The [redacted]. (Tr. (Reinman) at 266:1–267:16.).

Rather than focusing on the '506 Accused Multipipe Products, Dr. Lastra testified in hypotheticals and opined that FIFOs ***generally*** hold data to maintain workload as opposed to performing load balancing between pipelines, and that holding data actually works against load balancing, because it may imbalance the pipeline by trapping work in the FIFO. (Tr. (Lastra) 763:16-764:3 ("FIFOs are like in-boxes. So imagine that instead of a GPU, what you have are, say, four accountants, and each accountant has an in-box, and the accountant is processing a tax return. Now, I'll add another rule to the in-box, that you can't take work back. And once you have assigned it, it's done. So what can happen, and this happened in the systems that we built, is if you put too much work in the in-box, then one accountant may have extremely complex tax returns and so that accountant will be working past April 15, whereas maybe the other

[37] "FIFO" stands for "First-in, First-out." (JX-0001 at 3:8-10; *see also* Tr. (Reinman) at 266:5-9.). Dr. Reinman explained that a FIFO unit is "a buffer that will hold data," wherein the data "will leave the buffer in the same order in which it came in." (Tr. (Reinman) at 266:7-9.).

accountants have simple tax returns and aren't working.").).

Moreover, Dr. Lastra's testimony that was in fact directed to the accused was equivocal, and focused on theoretical circumstances where FIFOs might not serve the load balancing capability. (*Id.* at 764:4-6 ("So in these tiled, not all -- necessarily all tiled, but the , FIFOs actually ***can*** hurt.") (emphases added). Tellingly, and as Complainants pointed out, Dr. Lastra did not testify that the FIFOs in the do not balance the load. (*Id.*; CBr. at 62.). Dr. Lastra's testimony with regard to how FIFOs might ***theoretically*** hurt the load balancing in the is not persuasive.

Even assuming, *arguendo*, that the FIFOs might hurt load balancing under some circumstances, that does not undermine Dr. Reinman's testimony that they . This is enough for infringement as a matter of law. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1333 (Fed. Cir. 2013) (quoting *Bell Commc'n Research, Inc. v. Vitalink Commc'n Corp.*, 55 F.3d 615, 622-23 (Fed. Cir. 1995)) ("It is well settled that an accused device that 'sometimes, but not always, embodies a claim[] nonetheless infringes.'"); *cf. Paper Converting Mach. Co. v. Magna-Graphics Corp.*, 745 F.2d 11, 20 (Fed. Cir. 1984) ("Imperfect practice of an invention does not avoid infringement.").

Thus, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this additional claim limitation and infringe claim 2 of the '506 patent.

3. Claim 3 of the '506 Patent

a) "The graphics chip of claim 1 wherein each of said parallel pipelines further comprises: a z buffer logic unit; and a color buffer logic unit."

The record evidence in this Investigation demonstrates that the '506 Accused Multipipe Products include both a z and a color buffer logic unit module, which Respondents did not

dispute. (CX-1435 ( ) at 187, 299; CX-2229C ( ) at 74-76, 177-178; CX-2241C ( ) at 9, 26.). The nthesize into the z buffer logic unit recited in claim 3, while the synthesizes into an element that also buffers color. (Tr. (Reinman) at 267:22–272:14.).

Thus, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this additional claim limitation and infringe claim 3 of the '506 patent.

4. Claim 4 of the '506 Patent

a) "The graphics chip of claim 3 wherein said z buffer logic unit interfaces with said scan converter through a hierarchical Z interface and an early Z interface."

Evidence presented in this Investigation establishes that the z buffer logic unit in the '506 Accused Multipipe Products interfaces with a scan converter through a hierarchical and an early z interface, which Respondents did not dispute. (*See, e.g.*, CX-1435 ( ) at 81-82, 195-197, 219, 221; CX-2229C ( ) at 88; CX-2241C ( ) at 9, 26.). Specifically, the , which acts as the scan converter in the , interfaces with (part of the z buffer logic that is the hierarchical z buffer). (Tr. (Reinman) at 274:4-17.). In addition, the portion of that functions as the early z buffer interfaces with the scan converter through a . (*Id.* at 274:18–275:5.).

Thus, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this additional claim limitation and infringe claim 4 of the '506 patent.

5. Claim 5 of the '506 Patent

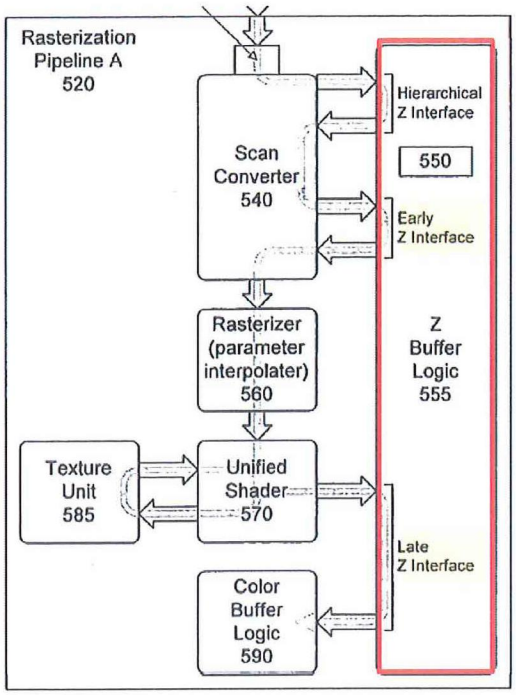
a) "The graphics chip of claim 3 wherein said z buffer logic unit interfaces with said unified shader through a late Z interface."

The record evidence demonstrates that that the z buffer logic unit in the '506 Accused Multipipe Products interfaces with a unified shader through a late z interface. (CX-1435 ( ); CX-2229C ( ).). Specifically, the , which functions as the interface between the unified shader and the late z interface . (Tr. (Reinman) at 275:14–277:16.).

Dr. Lastra opined that Dr. Reinman did not differentiate between the circuitry used for early Z and late Z in the Z buffer logic unit . (Tr. (Lastra) at 765:22–766:8.). According to Dr. Lastra, the early Z and late Z interfaces need to be separate, and the Z buffer logic unit needs to have separate and distinct circuitry for performing early Z and late Z testing. (*Id.*). For the reasons discussed below, Dr. Lastra's conclusion impermissibly narrows the scope of claim 5.

As depicted in the excerpt of Figure 5 reproduced below, both the early and late Z interfaces (highlighted in yellow below) share the same Z buffer logic unit **555** (in red below).

Figure No. 14: Figure 5 of the '506 Patent Depicting Early and Late Z Interfaces



(JX-0001 at Fig. 5 (excerpt) (annotated).).

Moreover, although the claims and specification of the '506 patent leave open the possibility as to whether the early and late Z testing is performed by the same exact logic or distinct logic within Z buffer logic **555**, it improper to read either of the two choices into the claim as a limitation. *Kara Tech. Inc. v. Stamps.com, Inc.*, 582 F.3d 1341, 1348 (Fed. Cir. 2009) ("The claims, not specification embodiments, define the scope of patent protection. The patentee is entitled to the full scope of his claims, and we will not limit him to his preferred embodiment or import a limitation from the specification into the claims.").

Thus, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this additional claim limitation and infringe claim 5 of the '506 patent.

6. Claim 8 of the '506 Patent

a) "The graphics chip of claim 1 wherein the unified shader is operative to . . . apply a programmed sequence of instructions to rasterized values and is operative to loop back to process operations for color shading and/or texture address shading."

Evidence adduced in this Investigation reflects that the unified shader in the '506 Accused Multipipe Products applies instructions to rasterized values and loops back to process color and/or texture operations. (CX-1435 ( ) at 26, 29-31, 36-38; CX-1490C ( ) at 14-15, 21, 27-28; CX-2229C ( ) at 16-17, 20-21, 27-28.). The synthesizes a loop back, (highlighted in yellow below), extending from the back to the unified shader. (Tr. (Reinman) at 277:17–280:6.).

Figure No. 15: Excerpt of Dr. Reinman's Source Code Diagram

(CDX-0006C (annotated).).

During the evidentiary hearing, Respondents' expert, Dr. Lastra did not dispute that the is operative to apply a programmed sequence of instructions to rasterized values. (Tr. (Lastra) at 766:11–767:24.). Nor did he dispute that there is a loopback of the

calculations that goes through the [redacted]. (*Id.*). Instead, he opined that the claimed loopback cannot go through the [redacted] and that the loop has to fully reside within the unified shader. (*Id.* [redacted].

Dr. Lastra's proposed additional limitation is not in the claims of the specification of the '506 patent and is thus improper. *Kara Tech.*, 582 F.3d at 1348 ("The claims, not specification embodiments, define the scope of patent protection."). Claim 8 only requires that "the unified shader . . . is operative loop back," which the [redacted] does by [redacted]. (Tr. (Reinman) at 279:8–280:6; CDX-0006C.).

For the reasons discussed above, Complainants have proven by a preponderance of evidence that the '506 Accused Multipipe Products meet this additional claim limitation and infringe claim 8 of the '506 patent.

E. Validity

1. Legal Standard

a) Generally

Patent claims are presumed valid. 35 U.S.C. § 282. A respondent that has raised patent invalidity as an affirmative defense must overcome the presumption by "clear and convincing" evidence of invalidity. *Checkpoint Sys., Inc. v. U.S. Int'l Trade Comm'n*, 54 F.3d 756, 761 (Fed. Cir. 1995). Further, as stated by the Federal Circuit in *Ultra-Tex Surfaces, Inc. v. Hill Brothers Chemical Co.*:

> when a party alleges that a claim is invalid based on ***the very same references*** that were before the examiner when the claim was allowed, that party assumes the following additional burden:
>
> When no prior art other than that which was considered by the PTO examiner is relied on by the attacker, he has the added burden[38] of overcoming the deference that is due to a qualified government agency presumed to have properly done its job, which includes one or more examiners who are assumed to have some expertise in interpreting the references and to be familiar from their work with the level of skill in the art and whose duty it is to issue only valid patents.

Ultra-Tex Surfaces, Inc. v. Hill Bros. Chem. Co., 204 F.3d 1360, 1367 (Fed. Cir. 2000) (emphasis added) (quoting *Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.*, 725 F.2d 1350, 1359 (Fed. Cir. 1984)).

b) Obviousness

Under 35 U.S.C. § 103(a), a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made" to a person having ordinary skill in the art. 35 U.S.C. § 103(a). The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." *Richardson-Vicks*, 122 F.3d 1476, 1479 (Fed. Cir. 1997) (citing *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 (1966)).

After claim construction, "[t]he second step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4)

[38] This is not an added burden of proof but instead goes to the weight of the evidence. *Sciele Pharma v. Lupin Ltd.*, 684 F.3d 1253, 1260-61 (Fed. Cir. 2012). New evidence not considered by the PTO may carry more weight than evidence previously considered by the PTO. (*Id.*).

secondary considerations of non-obviousness." *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1354 (Fed. Cir. 1999) (citing *Graham*, 383 U.S. at 17). The existence of secondary considerations of non-obviousness does not control the obviousness determination; a court must consider "the totality of the evidence" before reaching a decision on obviousness. *Richardson-Vicks*, 122 F.3d at 1483.

The Supreme Court clarified the obviousness inquiry in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 389 (2007). The Supreme Court said:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* and *Anderson's-Black Rock* are illustrative–a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.
>
> Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicit.
>
> * * *
>
> The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way. In many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature, will drive design trends. Granting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously

known elements, deprive prior inventions of their value or utility.

KSR, 550 U.S. at 417-19.

The Federal Circuit has since held that when a patent challenger contends that a patent is invalid for obviousness based on a combination of several prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007) (citations omitted).

> The TSM[39] test, flexibly applied, merely assures that the obviousness test proceeds on the basis of evidence--teachings, suggestions (a tellingly broad term), or motivations (an equally broad term)--that arise before the time of invention as the statute requires. As *KSR* requires, those teachings, suggestions, or motivations need not always be written references but may be found within the knowledge and creativity of ordinarily skilled artisans.

Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc., 520 F.3d 1358, 1365 (Fed. Cir. 2008).

2. None of the Asserted Claims of the '506 Patent Are Invalid as Obvious

a) Claims 1, 2, and 8 of the '506 Patent Are Not Obvious Over Papakipos (RX-0376) in Combination with Gibson (RX-0368)

U.S. Patent No. 6,532,013 issued on March 11, 2003, to Matthew N. Papakipos and others ("Papakipos"), from U.S. Patent Application Serial No. 09/585,809 filed on May 31, 2000. (RX-0376.). U.S. Patent No. 6,750,867 issued on June 15, 2004, to Cliff Gibson ("Gibson"), from U.S. Patent Application Serial No. 09/831,386, and claims priority to a foreign application that was filed on November 6, 1998. (RX-0368.).

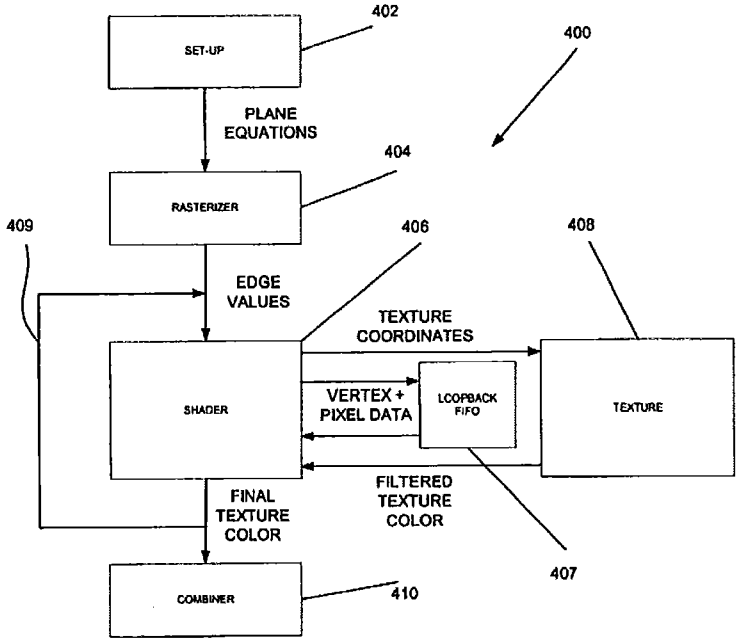
[39] TSM is an acronym that stands for teaching, suggestion, motivation.

Respondents alleged that Papakipos in view of Gibson renders obvious independent claim 1, and dependent claims 2 and 8 of the '506 patent. (RBr. at 26-27.).

There is no evidence that Papakipos or Gibson was considered by the PTO during the prosecution of the '506 patent. (*See* JX-0001.). There is also no dispute that Papakipos and Gibson are prior art to the '506 patent.

Papakipos describes a computer graphics pipeline that allows for repeated texture fetch and calculations in a single rendering pass, compared to the existing graphics pipelines that allowed only one texture fetch and texture calculation per rendering pass. (RX-0376 at 2:49-52.). In order to accomplish this, Papakipos describes a "shading module for performing the shading calculations" that is coupled to "a texture lookup module for retrieving texture information," as well as a feedback loop for the shading module that allows it to perform "additional shading calculations using the texture information from the texture lookup module." (*Id.* at 3:29-37.). As shown in Figure No. 16 (Figure 4 of the '506 patent), below, the shader module **406** is coupled to texture lookup module **408** as well as feedback loop **407** to allow shader module **406** to perform "another shading calculation using the texture information from the texture look-up module **408** in order to generate further output." (*Id.* at 5:13-16.).

Figure No. 16: Figure 4 of the '506 Patent



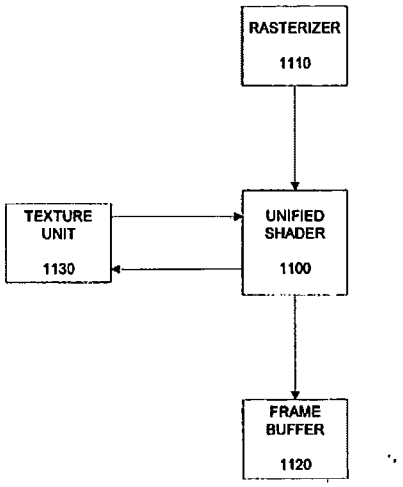
(JX-0001 at Fig. 4.).

With regard to Papakipos, the main dispute is whether Papakipos discloses the "unified shader" of claim 1. Claim 1 requires, in part, a graphics chip having a back-end that comprises multiple parallel pipelines, each of which has a "unified shader that is programmable to perform both color shading and texture shading." (JX-0001 at 14:30-42.). Conventional systems, in contrast, used separate shaders for "shading operations (i.e., color texture map and coordinate texture map or color shading operation and texture address operation)." (*Id.* at 6:53-57.). The unified shader of the '506 patent "is so named because the functions of a traditional color shader and a traditional texture address shader are combined into a single, unified shader" that "performs both color shading and texture address shading." (*Id.* at 6:49-53.). In other words, a "unified shader" is "a single shader circuit capable of performing color shading and texture

coordinate shading." (*Markman* Order Tr. at 13:10-24.)

As shown in Figure No. 17 (Figure 9 of the '560 patent) below, unified shader **1100** receives rasterized texture addresses and colors from rasterizer **1110**, performs "per-pixel shading calculations" on the values, and outputs the results to frame buffer **1120**. (JX-0001 at 6:47-49, 9:36-40.). Unified shader **1100** can also send "texture lookup requests" to texture unit **1130** as part of its calculations. (*Id.* at 9:40-42.).

Figure No. 17: Figure 9 of the '506 Patent

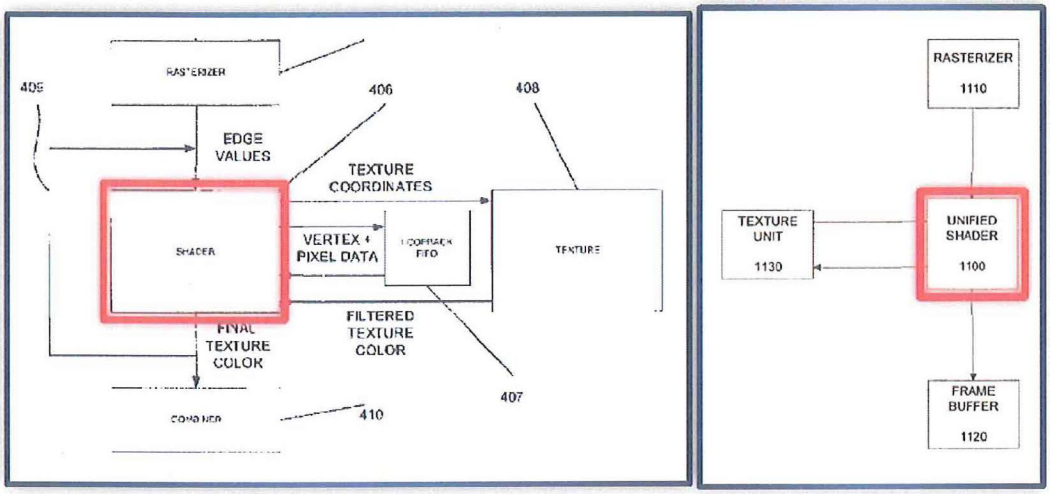


(JX-0001 at Fig. 9.)

Respondents failed to show by clear and convincing evidence that a person of ordinary skill in the art would recognize that Papakipos discloses the claimed unified shader—a single shader circuit capable of performing color shading and texture coordinate shading. Respondents asserted that the shader module **406** in Figure 4 of Papakipos is a unified shader because it receives rasterized color values and texture coordinates, works with a texture unit (texture lookup module **408**), and outputs final pixel values, just like unified shader **1100** of Figure 9 of the '506 patent. (RBr. at 20 (citing Tr. (Edwards) at 979:11–980:20); *id.* at 41 (citing RX-0376 at Fig. 1,

Fig. 4, 2:4-6, 2:63-64, 4:10-21, 5:18-27; JX-0001 at Fig. 9, 9:36-44).). Respondents contended that the similarities between Figure 4 of Papakipos and Figure 9 of the '506 patent, as shown below Figure No. 18, is evidence that Papakipos shader **406** behaves in the same manner as the unified shader **1100** of the '506 patent.[40] (*Id.*).

Figure No. 18: Comparison of Figure 4 of Papakipos and Figure 9 of the '506 Patent



RX-0376 (Papakipos), Fig. 4. JX-0001 ('506 Patent), Fig. 9.

(RX-0376 at Fig. 4; JX-0001 at Fig. 9.).

Respondents also relied on the specification of the '506 patent to argue that Papakipos shader module **406** performs the same functionality of the unified shader **1100** of the '506 patent. (*Id.* at 50.). However, the law disfavors using the invention against the inventor in this manner. *See, e.g., WL Gore & Associates, Inc. v. Garloc, Inc.*, 721 F.2d 1540, 1553 (Fed. Cir. 1981) ("To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the

[40] These figures are reproduced from page 20 of Respondent's Post-Hearing Brief, and include Respondents' annotations to the figures from the patents.

insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.").

The specification disclosed in Papakipos establishes that shader **406** is not a single shader circuit capable of performing color shading and texture coordinate shading. To begin with, the Papakipos shader **408** does not perform texture coordinate shading. Although Papakipos teaches that shader **408** can perform a "shading calculation . . . using the texture information in order to generate additional output," this shading calculation is not texture coordinate shading. (RX-0376 at 2:64-67, 5:4-12.). This shading calculation is instead described to include calculations that "diffuse output colors, fog output values, specular output colors, depth output values, texture color output values, a level of detail (LOD) value, and/or a Z-slope value." (*Id.* at 5:60-63.). As Complainants' expert, Dr. Wolfe, testified:

> Q: Now, are the -- are the different things here, fog output values, specular output colors, depth output values, texture color output values, level of detail value or a Z-slope value, are those operations on texture coordinates?
>
> A: No, none of those are operations on texture coordinates.
>
> Q: Are those color calculations?
>
> A: Most of them are color calculations. Others are things that are represented in the same data format as color that had been traditionally done in a color shader.

(Tr. (Wolfe) at 1414:25–1415:10.).

Nor does Papakipos' shader **406** perform texture coordinate shading by performing a "texture address calculation," as Respondents contended. (RBr. at 46-47; RX-0376 at Fig. 6 (block 602), 5:33-42.). Complainants' expert testified that texture address calculations are performed "during texture coordinate generation or during ordinary texture mapping." (Tr. (Wolfe) at 1378:15-19; *see also id.* at 1372:8-14 ("Texture mapping is simply the process of figuring out which part of a texture corresponds to which pixel we see on the screen."); Tr.

(Edwards) at 1221:8-12 (confirming that texture mapping can be done without performing texture coordinate shading).). Experts for both parties agreed that texture coordinate shading, by contrast, is an operation that modifies or changes already-existing texture coordinates. (Tr. (Edwards) at 1089:25–1090:21 ("So you have some texture coordinates, you do some arithmetic or something on them and you have new texture coordinates."), 1224:25–1225:20; Tr. (Wolfe) at 1374:8-23, 1377:14–1380:1.).

Papakipos instead teaches that texture module **408**, not shader **406**, performs the calculations that could possibly be used in texture coordinate shading. After shader **406** generates the texture coordinates, it sends those coordinates to texture module **408**. (RX-0376 at 5:7-8.). One function of texture module **408** is to "calculate an individual texture look-up" by performing mathematical computations. (*Id.* at 4:45-49, Table 1; Tr. (Wolfe) at 1413:14–1414:14.). Texture module **408** then sends texture information back to shader **406**. (JX-0001 at 5:4-12.). Therefore, to the extent that Papakipos discloses texture coordinate shading, texture module **408** performs the necessary shading calculation. (*See* Tr. (Wolfe) at 1416:9–1416:14 ("The color shading operations happen in shader **406**, and any more complicated texture operations happen over in texture unit **408**.").).

Papakipos does not disclose whether the texture module and shader module are on the same circuit as required by claim 1 of the '506 patent, or if they are on separate circuits, or even if each individual component is comprised of a single circuit or multiple circuits. (Tr. (Wolfe) at 1416:15-20, 1417:5-7.). Papakipos instead describes the shader and texture modules as "coupled to" each other as separate "logical modules."

> ***Coupled to the shading module is a texture lookup-module for retrieving texture information.*** Further, a feedback loop is coupled between an input and an output of the shading module for performing additional shading calculations using the

> texture information from the texture look-up module. Also included is a combiner module coupled to the output of the shading module for combining the output generated by the shading module. In one aspect of the present embodiment, at least ***a pair of texture look-up modules is coupled to a pair of shading modules which together constitute at least four logical modules.***

(RX-0376 at 3:28-42 (emphases added); *see also id.* at 4:12-17, 5:26-29.).

As Staff recognized, this "actually suggests that shading and texturing operations are performed by separate hardware components or circuits—shading is performed in a 'shading module' while texturing occurs in a 'texture look-up module.'" (SRBr. at 15-16 (citing RX-0376 at 3:29-32, 4:50-54).).

Papakipos, therefore, describes what the '506 patent refers to as a conventional system, where different shading operations are performed by different components. (JX-0001 at 6:53-57.). The testimony of Respondents' expert, Dr. Edwards, to the contrary is given limited weight because he did not correctly apply the definition of unified shader when reaching his conclusions. Specifically, a unified shader must be capable of performing the color shading and texture coordinate shading in a single circuit, but Dr. Edwards incorrectly understood that some of the color shading and texture coordinate shading operations of the unified shader could be performed by components outside of the unified shader circuit.

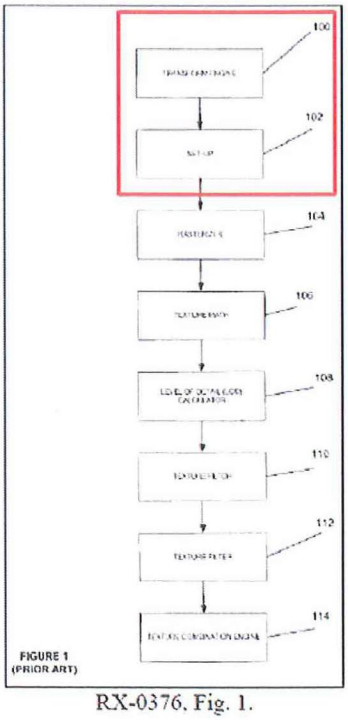
> Q: Well, let's -- let's go over both of those. First, all elements. Do you understand the construction provided by the Court for unified shader to mean that all elements in the single circuit that are involved in texture coordinate shading are also the elements in the circuit that are involved in color shading?
>
> A: Not all of them necessarily.
>
> * * *
>
> Q: Are all of your invalidity opinions based on your understanding of the Court's construction of unified shader?
>
> A: Yes.

(Tr. (Edwards) at 1280:11-17, 1280:23–1281:1; *compare Markman* Order Tr. 13:10-24.).

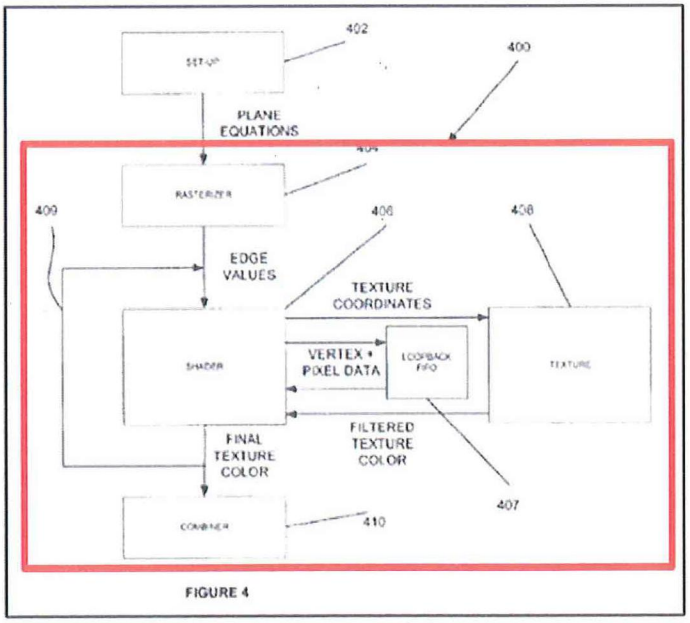
Complainants also asserted that Papakipos does not disclose the claimed "front-end in the graphics chip configured to receive one or more graphics instructions and to output a geometry." (CRBr. at 22.). Complainants argued that Respondents improperly mix-and-match different disclosures in Papakipos to satisfy the requirement of claim 1—the transform engine **100** and set-up module **102** in Figure 1 as the claimed "front-end" and other components in Figure 4 as the claimed "back-end." (*Id.* at 22-23.).

Complainants are correct that Respondents piece together different embodiments in Papakipos—the prior art embodiment of Figure 1 and an embodiment of the invention of Figure 4—to satisfy the separate front-end and back-end limitations of the '506 patent claim 1, as shown in Figure No. 19 below.

Figure No. 19: Figures 1 and 4 of Papakipos



RX-0376, Fig. 1.



RX-0376, Fig. 4.

(RBr. at 29, 31 (annotated by Respondents to identify the components in Papakipos alleged to satisfy the front-end limitation (Figure 1) and the back-end claim limitation (Figure 4)).).

This would normally be improper, as Respondents only relied on Papakipos' express teachings to disclose these limitations. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) ("The prior art reference – in order to anticipate under 35 U.S.C. §102 – must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'") (citation omitted). However, Papakipos teaches that "set up module **402**, rasterizer **404**, and combiner **410** operate in a conventional manner as set forth during reference to FIG. 1." (RX-0376 at 4:17-20.). In this instance, a person of ordinary skill in the art would understand the description of these modules in reference to Figure 1 applies equally to Figure 4.

Respondents conceded that Papakipos does not disclose parallel pipelines, and thus relied on Gibson for the "basic idea of using a parallel pipeline." (RBr. at 36 (quoting Tr. (Edwards) at 972:11-18), 38.) Respondents argued that when combined with Papakipos, Gibson discloses the claimed back-end with multiple parallel pipelines each having a unified shader. (*Id.* (quoting Tr. (Edwards) at 972:11-18); *see also id.* at 38.). Respondents did not rely on Gibson for disclosing the unified shader, or any part thereof. (*Id.* at 34-41.). As Papakipos does not disclose the unified shader, the combination of Papakipos with Gibson does not disclose the unified shader of claim 1.

Moreover, a person of ordinary skill in the art would not have a reason to combine Gibson with Papakipos, nor would such a person have a reasonable expectation of success in doing so. Gibson describes a method and apparatus for the real-time texturing or shading of three-dimensional images by dividing the image into sub-regions and allocating each region to a

separate rending device. (RX-0368 at 2:66–3:7, 3:42-45.). The rendering devices operate in parallel, with the outputs of each subsequently combined by tile interleaving and image display circuitry to form the final image. (*Id.* at 3:12-17, 4:4-10, 6:36-42.).

Complainants' expert, Dr. Wolfe, opined that "Gibson is an unusual architecture that's focused on speed at the expense of flexibility" and, in turn, "makes a lot of assumptions in order to have parallel pipelines." (Tr. (Wolfe) at 1418:19-22.). The pipeline in Papakipos takes one polygon, fills in all the pixels in the polygon, and then moves on to the next one. (*Id.* at 1418:25–1420:23.). In contrast, Gibson takes every polygon in advance, sorts them, builds tiles made up of pixels from different polygons, and then processes the tiles in parallel. (*Id.*; RX-0368 at 6:5-35.). Gibson can process multiple polygons at the same time because Gibson assumes they will all be treated the same way, and there is no shading program associated with each polygon. (Tr. (Wolfe) at 1418:25–1420:23.). Nothing in Gibson teaches how to transform Papakipos' linear per-polygon processing pipeline into a parallel multi-polygon processing pipeline, or vice versa.

Respondents did not address these difficulties in combining Papakipos with Gibson. Instead, Respondents argue that: (1) Gibson generally teaches parallel pipelines in graphic processors; (2) retrofitting Papakipos with parallel processing would have been obvious because the concept of parallel pipelines for electronic devices has been around since the 1960s; and (3) a person of ordinary skill in the art would have been motivated to add parallel processing to Papakipos because parallel processing reduces the overall processing time. (RBr. at 34-35 (citing RX-0368 at 7:8-13; Tr. (Edwards) at 971:7-17, 972:8-10, 973:14-20; Tr. (Wolfe) at 1440:1-13).)

Respondents failed to establish that implementing parallel processing in the Papakipos

graphics pipeline, or implementing parallel processing as claimed in the '506 patent, was common knowledge at the time of the invention. Respondents also failed to establish that a person of ordinary skill in the art would have had a reasonable expectation of success in applying parallel processing to Papakipos, or that Papakipos could be modified to include parallel processing based on the teachings of Gibson, in a way that meets the limitations of the '506 patent.

Respondents are correct that they do not have to prove that the Gibson system can be physically combinable with Papakipos. However, they are still required to establish that a person of ordinary skill in the art would have applied the teachings of Gibson to Papakipos to create the invention with a reasonable expectation of success. (RBr. at 37 (citing *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012)).). The unsupported testimony of Respondents' expert that doing so is "routine engineering" is not sufficient to meet their burden. (*See* Tr. (Edwards) at 972:24–973:13.). *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) (holding that conclusory expert testimony was not sufficient to establish obviousness).

Respondents failed to establish by clear and convincing evidence that claims 2 and 8, which depend on claim 1, are invalid as obvious for the same reasons as claim 1. *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1375 (Fed. Cir. 2013) (dependent claims cannot be obvious "where the base claim has not been proven invalid").

Accordingly, for the foregoing reasons, Respondents have failed to prove by clear and convincing evidence that claims 1, 2, and 8 of the '506 patent are rendered obvious by Papakipos in view of Gibson. Accordingly, claims 1, 2, and 8 are not invalid as obvious over Papakipos in combination with Gibson.

b) Claims 3 and 4 Are Not Obvious Over Papakipos (RX-0376) in Combination with Gibson (RX-0368) and Zhu (RX-0359)

U.S. Patent No. 6,697,063 was issued on February 24, 2004, to Ming Benjamin Zhu ("Zhu"), from U.S. Application Serial No. 08/978,491, and claims priority to a provisional application that was filed on January 3, 1997. (RX-0359.). Zhu was considered by the PTO during the prosecution of the '506 patent. (*See* JX-0001.). There is no dispute that Zhu is prior art to the '506 patent.

Respondents alleged that claim 3 of the '506 patent, which depends on claim 1, and claim 4 of the '506 patent, which depends on claim 3, are obvious in view of Papakipos over Gibson and Zhu. (RBr. at 53, 55.).

Claim 3 requires that the parallel pipelines comprise a z buffer logic unit and a color buffer logic unit, and claim 4 places more restrictions on the z buffer logic unit of claim 3. (JX-0001 at 14:46-53.). Zhu discloses a "high performance, high quality, and low cost 3D graphics rendering pipeline" that uses a z buffer logic unit (Z Buffering 1806) and a color buffer logic unit (Color Buffer 1403). (RX-0359 at 1:11-13, 34:50-55, 37:30-34, Figs. 14, 18.).

The parties disputed whether a person of ordinary skill in the art would have a reason to combine the teachings of Zhu with Gibson to add z buffer logic units and color buffer logic units to a parallel processing pipeline. Gibson and Zhu teach alternative methods of determining which parts of a polygon should be rendered on a screen, and Complainants argue that a person skilled in the art would choose one method or the other. (RX-0368 at 6:23-34; Tr. (Edwards) at 1248:1–1249:4.). Specifically, Gibson uses "ray-casting" that sorts the images front-to-back to determine which pixels are visible and thus should be rendered, whereas Zhu uses z buffering to render the visible fragments. (RX-0359 at 3:46-49; Tr. (Edwards) at 1248:1–1249:4.).

Complainants argued that a person of ordinary skill in the art would not replace Gibson's ray-casting with Zhu's z buffering system to take advantage of Gibson's parallel pipeline because the alternative methods are incompatible with each other. (CBr. at 30-32.). However, if such a person would have a reason to combine Papakipos with Gibson, a person of ordinary skill would have a reason to add Zhu to the combination as Papakipos itself discloses a z buffer logic unit. (RX-0376 at 4:20-27; Tr. (Wolfe) at 1424:10-15.). That said, a person of ordinary skill in the art would not have a reason to combine Papakipos with Gibson, as discussed above, so such a person would also not add Zhu to the proposed combination.

Respondents relied on Zhu for disclosing the unified shader of claim 1, or any part thereof. (*Id.*). Because Respondents failed to establish by clear and convincing evidence that the combination of Papakipos with Gibson discloses the unified shader, they have also failed to establish that the combination of Papakipos with Gibson and Zhu discloses the unified shader. *SynQor*, 709 F.3d at 1375 (Fed. Cir. 2013).

For the foregoing reasons, Respondents have failed to prove by clear and convincing evidence that claims 3 and 4 of the '506 patent are rendered obvious by Papakipos in view of Gibson and Zhu. Accordingly, claims 3 and 4 are not invalid as obvious over Papakipos in combination with Gibson and Zhu.

c) Claims 1, 2, and 8 Are Not Obvious Over Donham (RX-0142) in Combination with Gibson (RX-0368)

U.S. Patent No. 6,980,209 was issued on December 27, 2005, to Christopher D. S. Donham and others ("Donham"), from U.S. Application Serial No. 10/172,174 filed on June 14, 2002. (RX-0142.). Donham was considered by the PTO during the prosecution of the '506 patent. (*See* JX-0001.). There is no dispute that Donham is prior art to the '506 patent.

Respondents alleged that Donham in view of Gibson renders obvious independent claim 1, and dependent claims 2 and 8 of the '506 patent. (RBr. at 59.).

As it relates to claim 1 of the '506 patent, Donham discloses a graphics system with a pixel shader pipeline that can be scaled to perform increasingly large number of texture operations on individual polygons. (RX-0142 at 3:1-24, 6:25-24, Fig. 2.). For example, Figure 1 of Donham shows a graphics system with one pixel shader (30), and Figure 2 of Donham shows a graphics system with two pixel shaders (60 and 80) in series (shown side-by-side below in Figure No. 20). (*Id.* at 6:1-4, 10:1-13.)

Figure No. 20: Figures 1 and 2 of Donham

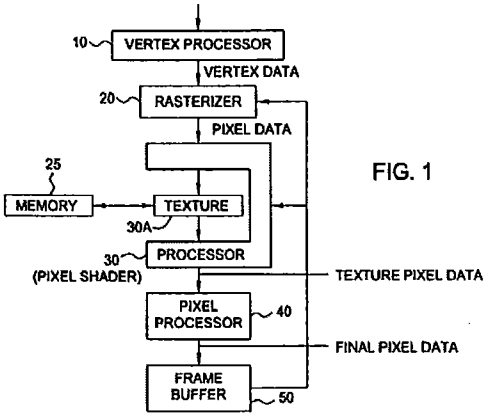


FIG. 1

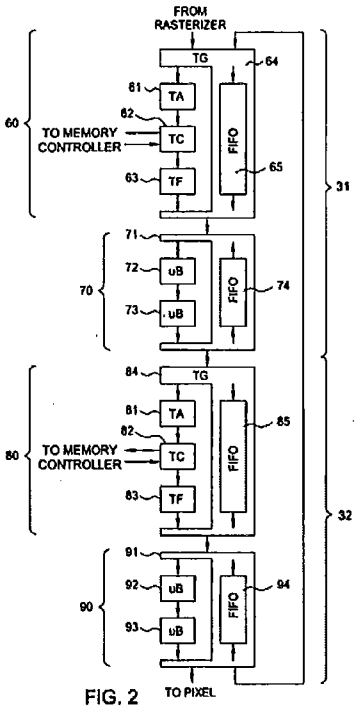


FIG. 2

(RX-0142 at Figs. 1, 2.).

In the Donham system, rasterizer **20** "generates pixel data" that is "indicative of the coordinates of a full set of pixels for each primitive, and attributes of each pixel (e.g., color

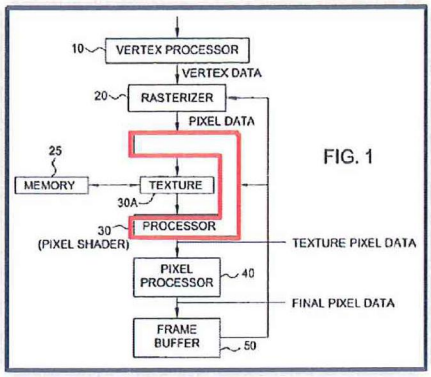
values for each pixel and values that identify one or more textures to be blended with each set of color values)." (*Id.* at 5:47-52.). Pixel shader **30** receives the pixel data and implements algorithms to process the pixels. (*Id.* at 6:1-23.).

The main dispute between the Parties is whether pixel shader **30** of Donham meets the "unified shader" limitations of claim 1. As described above, a "unified shader" is "a single shader circuit capable of performing color shading and texture coordinate shading." (*Markman* Order Tr. 13:10-24.). For the reasons discussed below, Respondents failed to demonstrate that Donham clearly and convincingly discloses the claimed "unified shader."

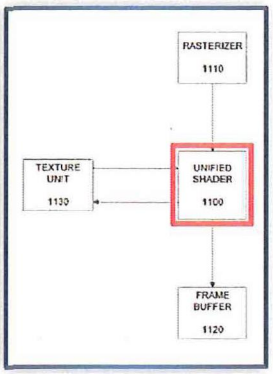
Respondents have not proven by clear and convincing evidence that a person of ordinary skill in the art would recognize that Donham discloses the claimed unified shader. Respondents asserted that the pixel shader **30** in Figure 1 of Donham is a unified shader because it receives texture and color information from rasterizer **20**, makes requests to and receives data from texture subsystem **30A**, and outputs final color values, just like unified shader **1100** of Figure 9 of the '506 patent. (RBr. at 22 (citing Tr. (Edwards) 1048:7–1049:18); *id.* at 66 (citing RX-0142 at Figs. 1, 2, 5, 6:45-52; JX-0001 at Fig. 9).). Respondents contended that the similarities between Donham Figure 1 and Figure 9 of the '506 patent, as shown below in Figure No. 21, is evidence that Donham pixel shader **30** behaves in the same manner as the Unified Shader 1100.[41] (*Id.*).

[41] The figures on this page are reproduced from page 22 of Respondent's Post-Hearing Brief, and include Respondents' annotations to the figures from the patents.

Figure No. 21: Comparison of Figure 1 of Donham and Figure 9 of the '506 Patent



RX-0142 (Donham), Fig. 1.



JX-0001 ('506 Patent), Fig. 9.

(RX-0142 at Fig. 1; JX-0001 at Fig. 9.).

The Donham specification establishes that pixel shader **30** is not a single shader circuit capable of performing color shading and texture coordinate shadings. As Respondents' expert, Dr. Edwards, conceded, Donham does not mention texture coordinate shading, or that pixel shader **30** modifies texture coordinates. (Tr. (Edwards) at 1236:6-15; *see also* Tr. (Wolfe) at 1428:24–1429:1-4.).

Respondents argued that Donham provides two examples of pixel shader **30** performing texture coordinate shading. Respondents pointed to Donham's statement that the microblender in pixel shader **30** is "capable of executing the mathematical operations required for efficient bump mapping."[42] (RBr. at 68 (quoting RX-0142 at 16:67–17:3).). Respondents pointed to the

[42] Respondents argued that bump mapping is an example of texture coordinate shading. (Tr. (Edwards) at 1068:16-23.). Complainants and Dr. Wolfe took inconsistent positions on whether bump mapping is a type of texture coordinate shading. For example, during the claim construction proceedings in this Investigation, Complainants and Dr. Wolfe asserted that the unified shader described in the '506 and '133 patents involves texture coordinate shading to accomplish, *inter alia*, bump mapping and indirect texturing. (Comp'ls Claim Br. at 24-25, 61-63; Declaration of Dr. Wolfe in Support of Complainants' Claim Construction Brief (CXM-0001) at ¶¶ 114-115, 117.). During the evidentiary hearing, Dr. Wolfe

math units in the "microblender" component of pixel shader **30**, which is depicted in Figure 5 of Donham (Figure No. 22 below), as performing "mathematical operations" that include the modification of texture coordinates. (*Id.* (citing Tr. (Edwards) at 1068:16–1069:2).). Dr. Edwards' conclusion that the math units modify texture coordinates is only with reference to Figure 5, and not with any support from the text of the specification. (Tr. (Edwards) at 1067:11–1069:2; *cf.* RX-0142 at 15:12-16, 16:38-43 (cited by Respondents at RBr. 69 to support its proposition, but these portions of Donham are silent on whether the math units modify texture coordinates).). Additionally, Figure 5 does not by itself teach the modification of texture coordinates.

Figure No. 22: Figure 5 of Donham

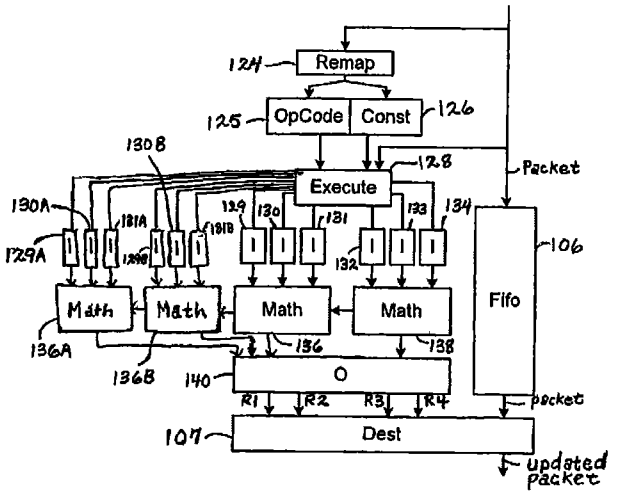


FIG. 5

---

testified for the first time that texture coordinate shading operations do not include calculating texture addresses, bump mapping, multi-texturing, or indirect texturing. (Tr. (Wolfe) at 1378:4–1380:1.) Complainants also raised for the first time in their Post-Hearing Reply Brief that based on testimony provided by Respondents' invalidity expert, Dr. Edwards, that bump mapping can be done without performing texture coordinate shading (Tr. (Edwards) at 1229:12-14, 1259:4-6, "bump mapping is not the same as texture coordinate shading." (CRBr. at 13, 16-17.). Dr. Wolfe's and Complainants' latter position is deemed waived abandoned, withdrawn, or waived. (*See* G.R. 7.2, 10.1.).

(RX-0142 at Fig. 5.).

Moreover, Donham does not disclose whether the components of pixel shader **30** are on a single circuit or on multiple circuits. As seen in Figure 2, which was reproduced earlier in this section (Figure No. 22, *supra*), the pixel shader comprises numerous components, including texture addressing stage **61**, texture cache **62**, texture filtering stage **63**, processor **64**, FIFO **65**, recirculating unit **71**, microblender **72**, microblender **73**, and FIFO **74**. (Tr. (Edwards) at 1264:22–1265:17; RX-0142 at 11:1-21.). Respondents' evidence that pixel shader **30** is a single circuit consists of comparisons with the unified shader of the '506 patent. (RBr. at 66.). The law, however, disfavors using the invention against the inventor in this manner. *WL Gore & Associates*, 721 F.2d at 1553.

As with Papakipos, Respondents argued that their reliance on Gibson is only for the "basic idea of using a parallel pipeline" that, when combined with Donham, disclose a graphics back-end that comprises multiple parallel pipelines each having a unified shader. (RBr. at 62 (quoting Tr. (Edwards) at 953:24–954:2).). Respondents did not rely on Gibson for disclosing the unified shader, or any part thereof. (*Id.* at 34-41.). As Donham does not disclose the unified shader, the combination of Donham with Gibson does render claim 1 of the '506 obvious.

Moreover, a person of ordinary skill in the art would not have a reason to combine Gibson with Donham, for the same reasons such a person would not combine Gibson with Papakipos. (*See id.* at 62-63 ("[T]he exact same motivations to combine, and the same supporting disclosures of Gibson, that were applicable for Papakipos . . . which are hereby incorporated by reference, are similarly applicable for the combination of Donham and Gibson.").)

Respondents failed to establish by clear and convincing evidence that claims 2 and 8,

which depend on claim 1, are invalid as obvious for the same reasons as claim 1. *SynQor*, 709 F.3d at 1375 (dependent claims cannot be obvious "where the base claim has not been proven invalid").

Thus, for the foregoing reasons, Respondents have failed to prove by clear and convincing evidence that claims 1, 2, and 8 of the '506 patent are rendered obvious by Donham in view of Gibson. Accordingly, claims 1, 2, and 8 are not invalid as obvious over Donham in combination with Gibson.

d) Claims 3 and 4 Are Not Obvious Over Donham (RX-0142) in Combination with Gibson (RX-0368) and Zhu (RX-0359)

Respondents relied on Zhu to disclose the z buffer logic unit and color buffer logic unit of claims 3 and 4 of the '506 patent, in the same way as described in relation to Papakipos. (RBr. at 71 ("Dr. Edwards relies on the exact same disclosures in Zhu in support of his obviousness opinions for both the Papakipos and Donham primary references.").). Similarly, Respondents relied on the same motivation to combine Zhu with Donham and Gibson as with Papakipos and Gibson. (*Id.* at 71-72 (citing Tr. (Edwards) at 1080:7–1081:6 ("Q: So can you tell us what the motivation to combine is for Zhu with Donham and Gibson? A: So it's the same motivation that I explained for Papakipos, with Gibson and Zhu.")).).

The conclusions reached with Papakipos apply here. If a person of ordinary skill in the art would have a reason to combine Dunham with Gibson, the person would also have a reason to add Zhu to the combination. However, such a person would not have a reason to combine Dunham with Gibson, so such a person would not add Zhu to the proposed combination. Respondents also do not contend that Zhu discloses a unified shader as required by claim 1, or any part thereof.

Because Respondents failed to establish by clear and convincing evidence that the combination of Donham with Gibson discloses the unified shader, they have also failed to establish that the combination of Donham with Gibson and Zhu discloses the unified shader. *SynQor*, 709 F.3d at 1375 (Fed. Cir. 2013).

For the foregoing reasons, Respondents have failed to prove by clear and convincing evidence that claims 3 and 4 of the '506 patent are rendered obvious by Donham in view of Gibson and Zhu. Accordingly, claims 3 and 4 are not invalid as obvious over Donham in combination with Gibson and Zhu.

VIII. U.S. PATENT NO. 7,796,133

A. Overview of Infringement

Complainants have alleged that the Multipipe and Singlepipe Accused Products ("the '133 Accused Products") infringe claims 1 and 3 of the '133 patent. (CPBr. at 63-70; CBr. at 73-91.). Complainants and Respondents have stipulated that the following are representative of the '133 Accused Products that Complainants have accused of infringing the asserted claims of the '133 patent.

Chart No. 15: Multipipe and Singlepipe Accused Products

Accused Vizio Products covered by Representative Product	Vizio Rep. Product	System Prod. Category	Commercial Name	Graphics Processor Model Name
All accused Vizio products that contain a		SOC		
All accused Vizio products that contain a		SOC		

Accused Vizio Products covered by Representative Product	Vizio Rep. Product	System Prod. Category	Commercial Name	Graphics Processor Model Name
All accused Vizio products that contain a		SOC		
All accused Vizio products that contain an		SOC		

(JX-0011C at 1-4.).

For the same reasons discussed with regard to the '506 patent in Section VII.B, *supra*, there is no dispute that the incorporated into Respondents MediaTek and SDI's SoCs accurately describe the structure, function, and operation of the '133 Accused Products. In addition, the evidence reflects that the '133 Accused Products all function the same way for purposes of determining infringement. (Tr. (Reinman) at 280:15-25.).

Based on the [redacted], and evidence adduced in this Investigation, the '133 Accused Products do not infringe the asserted claims of the '133 patent.

B. Relevant Claim Terms

The following constructions of the claim terms recited in the asserted claims of the '133 patent have been agreed upon by the parties or adopted by this Court.[43]

Chart No. 16: Constructions of Claim Terms Relevant to the '133 Patent

Claim Term	Construction
"unified shader" (claims 1 and 3)	A single shader circuit capable of performing color shading and texture coordinate shading. (*Markman* Order Tr. at 13:10-24.).
"rasterizer" (claim 1)	Circuit that generates texture coordinates and color values for a block of pixels. (*Id.* at 14:6-13.).
"packet" (claim 1)	Plain meaning, such as data bundle containing texture, coordinate and color value information for a block of pixels. (*Id.* at 21:5-17.).
"shading processing mechanism" / "said shading mechanism" (claim 1)	Plain meaning, the structure corresponding to the "shading processing mechanism" is recited in the claim. (*Id.* at 21:18–22:12.). This is not a means-plus-function limitation.

C. The '133 Accused Products Do Not Infringe Claims 1 and 3 of the '133 Patent

1. Claim 1 of the '133 Patent

a) "A unified shader comprising"

For the same reasons discussed in Section VII.D.1(f) with respect to the "unified shader"

[43] The Parties disputed the meaning of additional claim terms recited in claims that have been terminated from this Investigation. Those terms are not included in Chart No. 15.

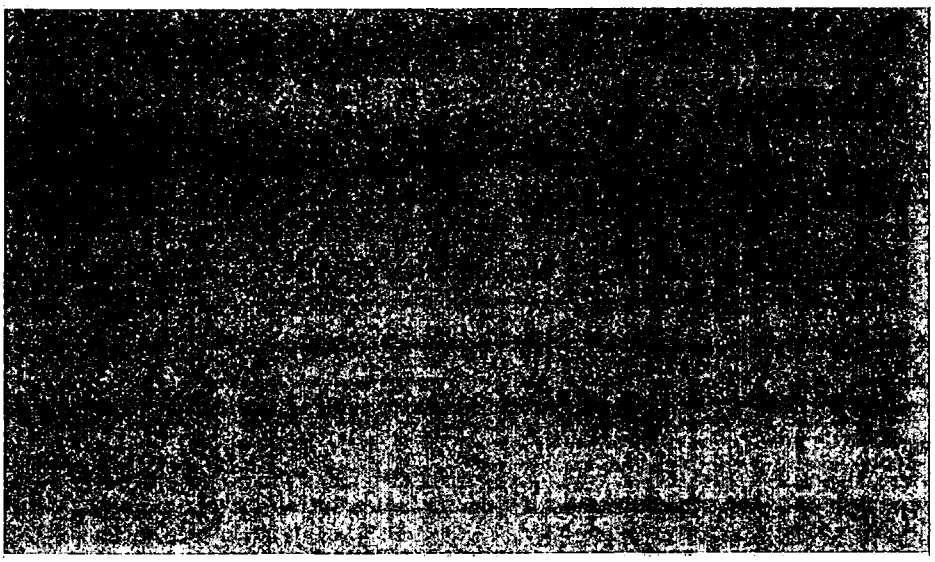
limitation of claim 1 of the '506 patent, Complainants have proven by a preponderance of evidence that the '133 Accused Products include a unified shader in the form of an [redacted] and meet the preamble of claim 1 of the '133 patent. (*See* Section VII.D.1(f).).

b) "an input interface for receiving a packet from a rasterizer"

The evidence adduced in this Investigation fails to establish that the [redacted] contains an input interface for receiving a packet from a rasterizer. The term "rasterizer" was construed to mean a "circuit that generates texture coordinates and color values for a block of pixels." (*Markman* Order Tr. at 14:6-13.). A "packet" was construed to mean a "data bundle containing texture, coordinate and color value information for a block of pixels." (*Id.* at 21:5-17.).

Each [redacted] includes a [redacted] (in yellow below) that performs [redacted] to generate and output rasterized color values and texture coordinates for a block of pixels. (*Id.* at 283:6-15; CDX-0006C; CX-1435C.0038.). The [redacted] contains a [redacted] (in green below), which receives the rasterized color values and texture coordinates from the [redacted] (in red below). (Tr. (Reinman) at 284:1-20; CDX-0006C; CX-1435C.0037.).

Figure No. 23: Dr. Reinman's Source Code Diagram Showing a "Rasterizer"



(CDX-0006C (annotated).).

Respondents did not dispute that the color values and texture coordinates to the . (RRBr. at 39-40.). Dr. Lastra's testimony, and technical documents and source code, corroborate Dr. Reinman's opinion that the is a rasterizer that rasterized values to the . (Tr. (Lastra) at 771:6–772:8 (Dr. Lastra explaining that the can generate); CX-1435C.0038 ( ); CX-1435C.0223 ( )

).

At the center of the Parties' dispute is whether the : (1) operates on a "block of pixels"; and (2) sends a "packet," i.e., "data bundle containing . . . information for a block of pixels." (Tr. (Reinman) at 281:24–285:17; Tr. (Lastra) at 771:24–772:4.). For the reasons discussed below, Complainants failed to demonstrate that the accused satisfies these claim limitations.

With respect to the "block of pixels" limitation, Dr. Lastra opined that the does not meet the rasterizer element because rather than receiving a task to generate texture coordinates and color values for a block of pixels as described in the '133 patent, the . (Tr. (Lastra) at 771:10-20

(emphases added), 772:4-8

(emphasis added).).

Complainants argued that "[n]othing in the construction of the term 'rasterizer' states that texture coordinates and color values need to be generated '***together***'" or requires that a circuit that generates texture coordinates and color values for a block of pixels must generate all of the texture coordinates and color values for that block ***at the same time***." (CBr. at 75 (emphases added) (citing Tr. (Lastra) at 771:6-13; RPBr. at 66).). However, as Respondents contended, Complainants' arguments miss the point. As Dr. Lastra explained, the issue is not whether the for a block of pixels but rather

whether the [redacted] ***operates on a block of pixels at all,*** as required by the claim construction. (Tr. (Lastra) at 771:9-20.). Dr. Lastra testified that the [redacted]. (*Id.*).

Complainants also contended that Dr. Lastra's testimony that texture coordinates and color values need to be generated "***together***" directly contradicts the '133 patent specification's disclosure that the rasterizer can generate texture addresses (i.e., texture coordinates) and color values ***in any order***. (CBr. at 75 (citing JX-0003 at 5:11-14).). However, the rest of this sentence to which Complainants cited indicates that the rasterizer of the '133 patent "generates a texture address (tc) and rasterization color (rc) in any suitable format and order at a rate of one pixel ***quad*** (a quad is a ***2×2 tile of pixels***) every clock," i.e., a block of pixels. (JX-0003 at 5:11-14.).

Additionally, Complainants asserted that an embodiment of the '133 patent describing a rasterizer that only generates two texture coordinates and two color values associated with one pixel of the block of pixels per clock cycle contradicts Dr. Lastra's opinion that all of the texture coordinates and color values for a block of pixels must be generated ***at the same time***. (CBr. at 76 (citing JX-0003 at 8:52-53).). This example of texture operation before packet transmission is inapposite and fails to support Complainants' assertion for at least two reasons.

First, nothing in the cited passage discloses that the two texture coordinates and two color values generated for that one pixel alone are outputted to the unified shader, that is, that they are not bundled with texture coordinates and color values generated for other pixels before being sent to the unified shader as a "packet." In fact, the specification repeatedly discloses that: (1) "[a]s data for ***each block of pixels*** is received from the rasterizer, a 'control token' is generated" (JX-0003 at 6:38-40) (emphasis added); (2) "[t]he control token contains a small amount of

information describing ***this block of pixels***" (*id.* at 6:40-41) (emphasis added); and (3) "[r]asterizer **400** generates packets of data containing information for ***a block of 16 pixels (4 quads)***" (*id.* at 6:48-49) (emphasis added). Second, as defined above, the "rasterizer" recited in claim 1 was construed to mean a "circuit that generates texture coordinates and color values for a ***block of pixels***." (Markman Order Tr. at 14:6-13.). That the specification also includes embodiments that may involve the transmission of texture coordinates and color values for a single pixel is irrelevant.

Tellingly, the original claim construction dispute centered on whether the "packet" must contain information for "16 pixels" (Respondents' proposed construction) or "a block of pixels" (Complainants and Staff's proposed construction). (*See, e.g.*, Comp'ls Claim Br. at 69.). Thus, the Parties and Staff agreed that a packet must contain information for ***multiple pixels***. (*See id.* at 70 ("the specification is not silent regarding the fact that the packets described in the '133 patent contain texture coordinate and color value information ***for pixels***."). None of the Parties argued that a "packet" should be construed to encompass a single value for a single pixel, [redacted]. (*See id.*).

With regard to the "packet" limitation, the adopted construction of a "packet" requires a "data bundle," not [redacted]. As discussed immediately above with respect to the "block of pixels" limitation, Dr. Lastra persuasively testified that the [redacted].

(*Id.* at 771:21–772:8.).

For the reasons discussed above, Complainants have failed to prove by a preponderance of evidence that the '133 Accused Products meet this limitation recited in claim 1 of the '133 patent.

c) "a shading processing mechanism configured to produce a resultant value from said packet by performing one or more shading operations"

For the reasons described above in Section VIII.C.1(b), the SoCs containing an [redacted] do not meet this limitation, as the alleged "shading processing mechanism" does not receive a "packet," and thus cannot produce a "resultant value from said packet."

Accordingly, Complainants have failed to prove by a preponderance of evidence that the '133 Accused Products meet this limitation recited in claim 1 of the '133 patent.

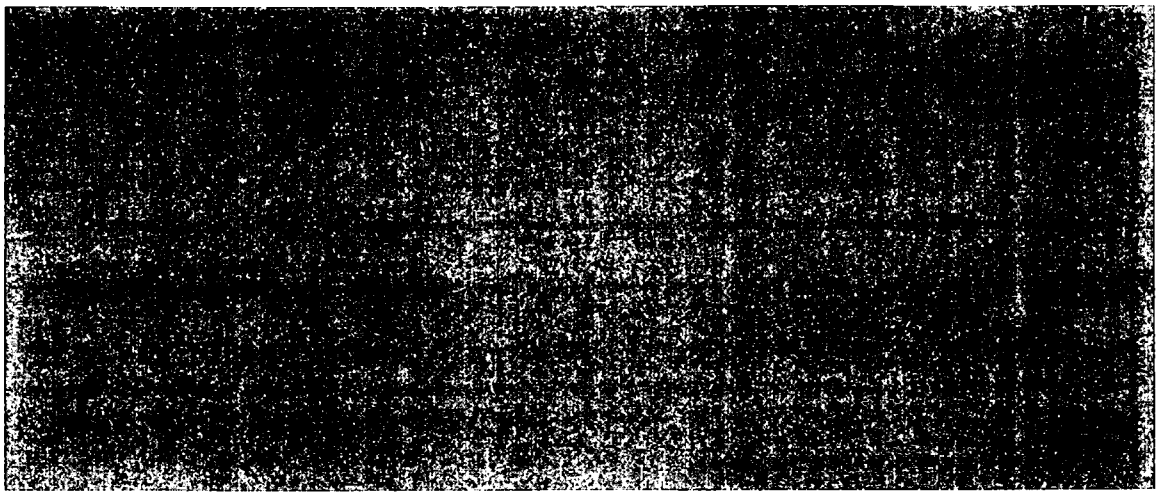
d) "wherein said shading operations comprise both texture operations and color operations and comprising at least one ALU/memory pair operative to perform both texture operations and color operations wherein texture operations comprise at least one of: issuing a texture request to a texture unit and writing received texture values to the memory"

Evidence presented in this Investigation fails to demonstrate that the [redacted] comprises at least one ALU/memory pair operative to perform both color operations and the recited texture operations. (Tr. (Reinman) at 288:9–294:19.).

With regard to the ALU/memory pair limitation, Complainants' expert, Dr. Reinman, opined that the [redacted] (in red below), and [redacted] (in purple below) correspond to the SRAM, ALU, and control disclosed in Figure 2 of the '133 patent, and that these components together constitute the ALU/memory pair recited in this limitation. (Tr. (Reinman) at 291:14-21 ("The ALU/memory pair is the combination of [redacted], that's the ALU, the [redacted], that's the memory side. And then the pairing is enabled by the [redacted]. That's orchestrating the interaction between the ALU and

the memory that allows them to operate together on a common color shading or texture coordinate shading operation.").).

Figure No. 24: Comparing Dr. Reinman's "ALU/Memory Pair" with Figure 2 of the '133 Patent



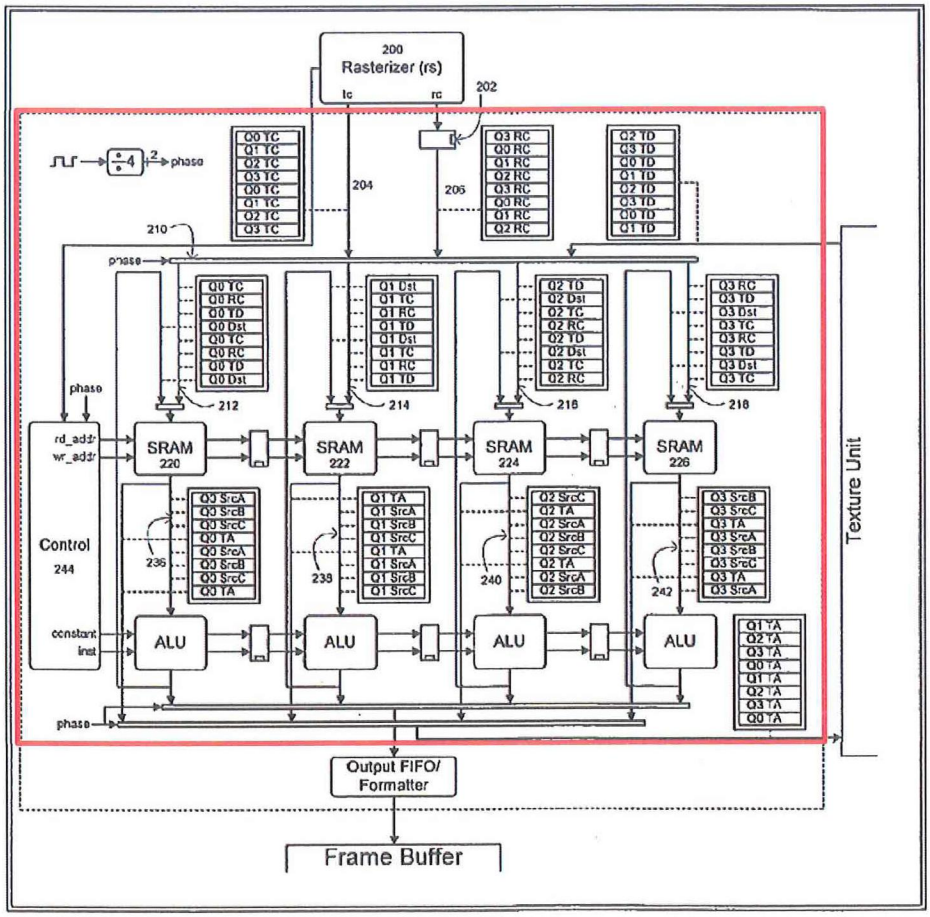
(CDX-0006C (annotated); JX-0003 at Fig. 2 (annotated).).

Dr. Reiman explained that: (1) the [redacted] (Tr. (Reinman) at 290:13–293:6; CX-1435C.0209-11); (2) the [redacted] (Tr. (Reinman) at 293:22–294:10; CDX-0006C); and (3) the [redacted] (Tr. (Reinman) at 293:7-21, 298:1–300:14; CDX-0006C).

As Dr. Lastra, Respondents' expert, pointed out, Dr. Reinman's ALU/memory pair (in

red below) essentially includes the entire unified shader architecture of the '133 patent, which is shown in Figure No. 25 (Figure 2 of the '133 patent), below. (Tr. (Lastra) at 778:9-19 ("So comparing Dr. Reinman's ALU to the '133 patent, can you identify on this figure, which is figure 2 from the '133 patent, what Dr. Reinman claims is the ALU? A: What I've done is identified in red -- in a red box what Dr. Reinman has -- the equivalent in the '133 patent, figure 2 of what Dr. Reinman has identified as an ALU/memory pair, which is essentially the ***whole processor***.") (emphasis added).

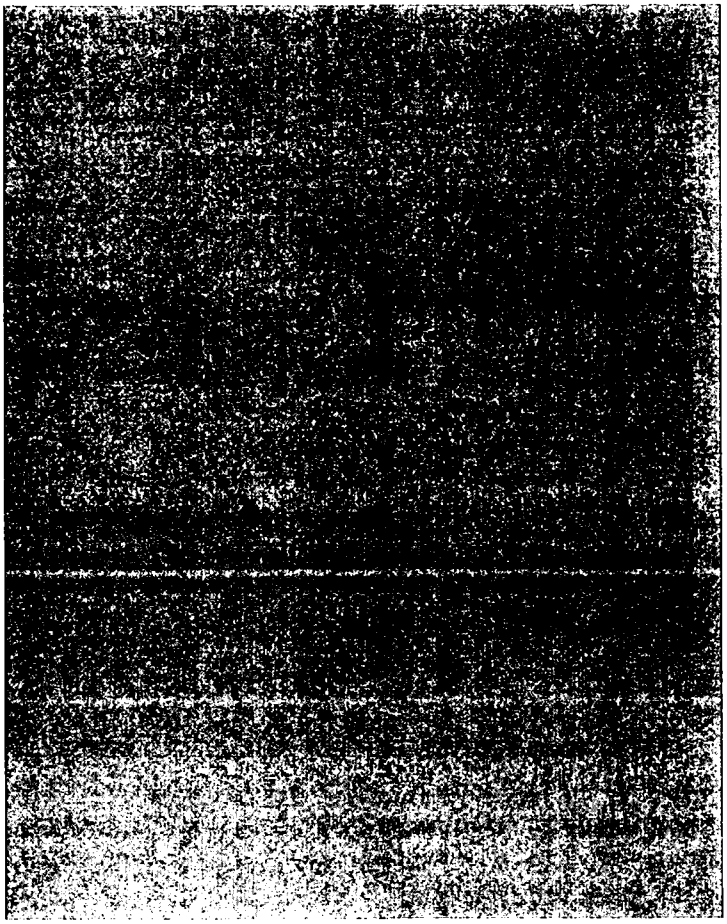
Figure No. 25: Figure 2 of the '133 Patent



(JX-0003 at Fig. 2 (annotated).).

Instead of identifying "an ALU/memory pair," Dr. Reinman identified an entire processor—the entire alleged "unified shader" itself—including [redacted], as shown in Figure No. 26 below. (Tr. (Lastra) at 778:9-19; (Tr. (Reinman) at 190:16–191:7 (Q: What are the exemplary elements of the ***unified shader*** architecture in the '133 patent? A: So there's three key elements here. We have got the computational resources, labeled here as ALU. We have the memory, labeled here as SRAM, and we've got the control that orchestrates and allows these components to act as a pair, which is the control.") (emphasis added).).

Figure No. 26: Comparing Dr. Reinman's "ALU/Memory Pair" With Dr. Reinman's Unified Shader

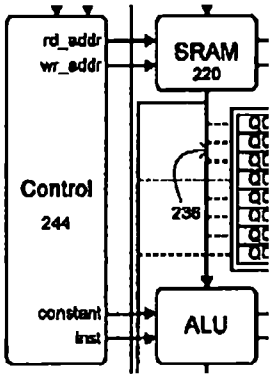


(CDX-0006C (annotated).).

The inclusion of the control resource in the ALU/memory pair is not consistent with the specification and claims of '133 patent. To begin with, the '133 patent claims as ***separate and distinct elements*** an "ALU" (claim 1) (*id.* at 11:49-64 ("A unified shader comprising . . . a shading processing mechanism . . . comprising at least one ALU/memory pair") and "control logic" (claim 6, dependent on claim 1) (*id.* at 12:9-14 ("The unified shader of claim 5 further comprises control logic . . . ."). Reading the control logic limitation recited in claim 6 into the ALU/memory pair limitation recited in claim 1 would render the control logic limitation superfluous. *Dig.-Vending Servs. Int'l, LLC v. Univ. of Phx., Inc.*, 672 F.3d 1270, 1275 (Fed. Cir. 2012) (quoting *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006)) ("If 'registration server' were construed to inherently contain the 'free of content managed by the architecture' characteristic, the additional 'each registration server being further characterized in that it is free of content managed by the architecture' language in many of the asserted claims would be superfluous. This construction is thus contrary to the well-established rule that 'claims are interpreted with an eye toward giving effect to all terms in the claim.'"). Thus, Dr. Reinman's "ALU/memory pair," which includes the , contradicts how the '133 patent describes these discrete components and illustrates the multiple ALU/SRAM pairs as separate from the control element.

Moreover, while the '133 patent does not disclose that an ALU/memory pair cannot include any control circuitry, the ALU/memory pairs described in the specification explicitly state that the ALUs do not contain control capability. (*See* JX-0003 at 9:26-36 ("No flow control is needed for this ALU . . . ."); *see also id.* at Fig. 7.). Specifically, the '133 patent expressly describes and depicts the "control" as separate from its "ALU" and "SRAM."

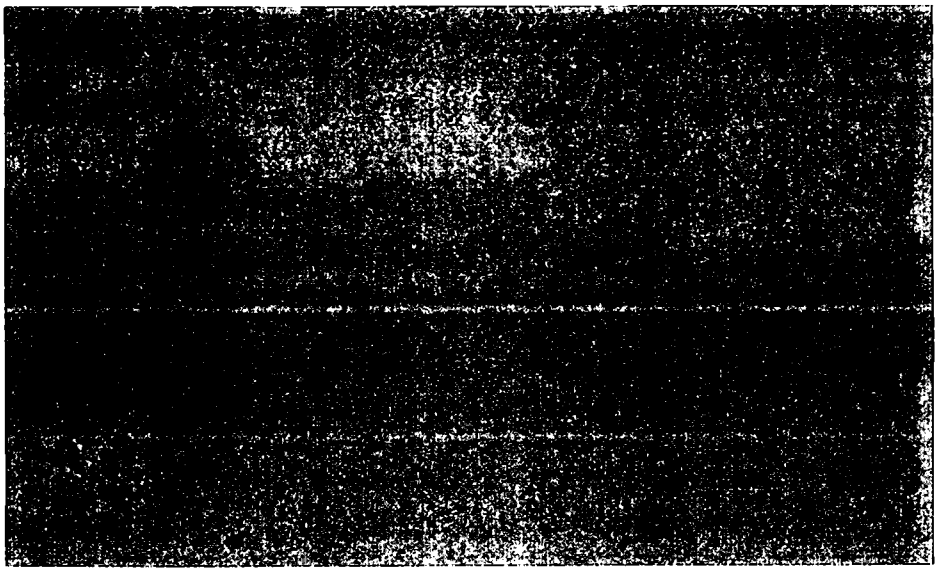
Figure No. 27: Excerpt of Figure 2 of the '133 Patent



(JX-0003 at Fig. 2.).

With respect to the "texture operations compris[ing] at least one of . . . issuing a texture request to a texture unit" limitation, Dr. Reinman testified that the [redacted] (in orange below). (Tr. (Reinman) at 297:1-25; CDX-0006C; CX-1435C.0037-8.).

Figure No. 28: Dr. Reinman's Source Code Diagram Showing a "Texture Unit"



(CDX-0006C (annotated).).

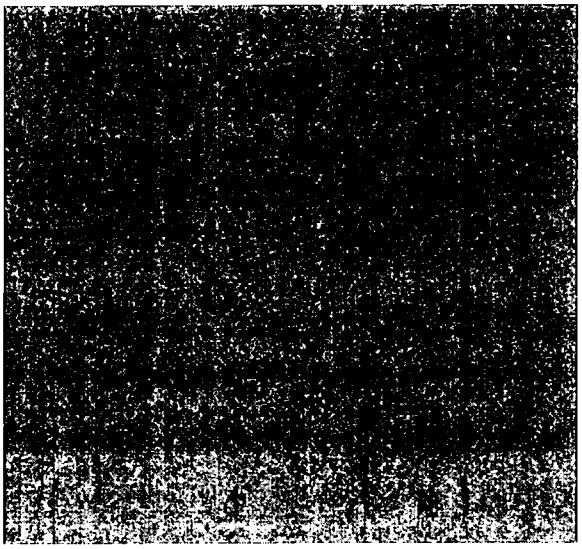
Based on Dr. Reinman's testimony, Complainants argued that the [redacted] (in purple above) of the ALU/memory pair issues [redacted] by sending a [redacted] (in yellow above), to the [redacted] (in yellow above), to the [redacted]. (Tr. (Reinman) at 298:1-4, 299:4-14, 618:11-23, 659:16–661:9, 810:6–811:17; CDX-0006C.). As discussed directly above, the [redacted] was found not to be a part of the ALU/memory pair. Thus, this aspect of Complainants' argument fails.

Referring to the illustration below (Figure No. 29), Dr. Reinman also testified that when the [redacted].[44] (Tr. (Reinman) at 307:23–308:8, 338:22–341:4, 1312:8–1316:12.).[45]

[44] In Respondents' MIL No. 4 (Motion Docket No. 1044-058 (Nov. 3, 2017)) and Motion to Strike (Motion Docket No. 1044-070 (Dec. 22, 2017)), Respondents asserted that Dr. Reinman's [redacted] was untimely disclosed and exceeded the scope of Complainants' infringement contentions, respectively. Both motions were denied. (*See* Pre-Hearing Tr. at 47:12-13; Order No. 62 (Apr. 12, 2018).).

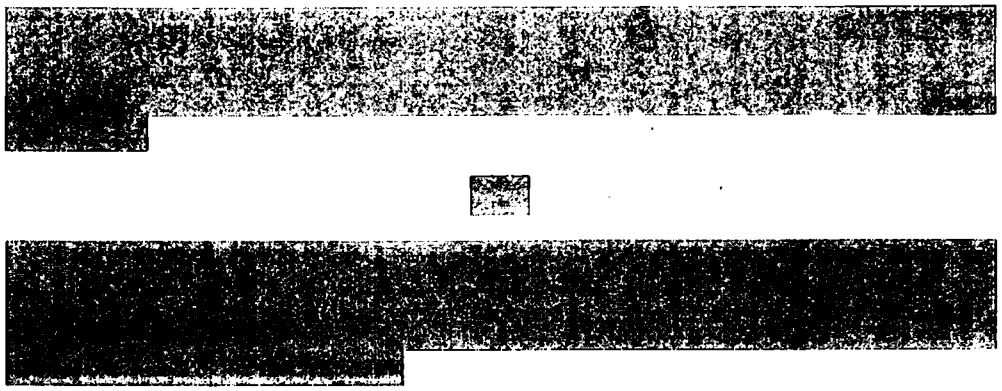
[45] Complainants raised the same [redacted] arguments for the "unified shader" limitation recited in claim 1 of the '506 patent. (*See* CBr. at 54-57.). These arguments were not discussed in the analysis of that claim because claim 1 of the '506 only requires a unified shader "programmable to perform texture shading," and does not specifically require that the unified shader "issue texture requests to a texture unit," as is the case with claim 1 of the '133 patent. For this reason, Complainants' [redacted] theory is only discussed here, in the context of claim 1 of the '133 patent.

Figure No. 29: Depiction of Dr. Reinman's [redacted] Theory



(CDX-0100C.101.).

Dr. Reinman based his testimony, *inter alia*, on [redacted].



(CBr. at 84-85 (emphases in original) (quoting CX-1435C.0204, 0223); Tr. (Reinman) at 338:22–341:4, 1312:8–1316:12.).

However, the text upon which Dr. Reinman relied refutes his testimony and supports Respondents' **assertion that in the [redacted], the texture request received by the [redacted] is still issued by the [redacted]. (CX-1435C.223 [redacted]**

[redacted]

[redacted] (emphases added).). This is also corroborated by ARM's corporate representative, Mr. Larri, who explained the [redacted] as follows:

[redacted]

(Tr. (Larri) at 669:9–670:25 (emphases added).

Mr. Larri also provided the following testimony with regard to the

(*Id.* at 656:22–657:11 (emphasis added).).

Mr. Larri's testimony was corroborated by Dr. Lastra. (Tr. (Lastra) at 740:19-24 ("Q: Do you agree with Dr. Reinman that the may issue ? A: No. The can't issue . Under some conditions, and I think others went through this, . . . the .") (emphasis added).).

In addition, Dr. Reiman opined that the does not modify the

value provided by the

(Tr. (Reinman) at 298:12–300:14, 307:23–308:8.).

While Mr. Larri confirmed that the

(*see, e.g.*, Tr. (Larri) at 664:13-20), he explained that a

(*id.* at 657:8-14). Mr. Larri clarified that

(*Id.* at 661:19–662:1.).

Moreover, Mr. Larri carefully distinguished

. He specified that

which he testified can

. (*Id.* at 669:1-8; *see also id.* at 668:12-20

).).

Therefore, the evidence weighs against a finding that in the

, the ALU/memory pair issues texture lookup requests to the texture unit.

With regard to the "texture operations compris[ing] at least one of . . . writing received texture values to the memory" limitation, Complainants argued in their Pre-Hearing Brief that

[redacted] (CPBr. at 67 (citations omitted).). Complainants did not raise or discuss this argument in their Initial Post-Hearing Brief. Thus, it is deemed waived. (*See* Ground Rule 10.1.). In their Initial Post-Hearing Brief, Complainants simply maintained that the ALU/memory pair need only perform one of the examples of texture operations. (CBr. at 86.). That assertion was not raised in Complainants' Pre-Hearing Brief and is similarly deemed abandoned or withdrawn. (*See* Ground Rule 7.2.).

For the foregoing reasons, Complainants have failed to prove by a preponderance of evidence that the accused ALU/memory pair issues a texture request to a texture unit or writes received texture values to the memory. Accordingly, the '103 Accused Products do not meet this limitation recited in claim 1 of the '133 patent.

e) "wherein the at least one ALU is operative to read from and write to the memory to perform both texture and color operations"

The evidence adduced in this Investigation fails to establish that at least one ALU is operative to read from and write to the memory to perform both texture and color operations. For the reasons discussed in Section VIII.C.1(d) above, neither the ALU nor the memory of the ALU/memory pair issues a texture request to a texture unit. Moreover, Complainants did not advance any meaningful arguments with regard to whether the accused ALU/memory pair writes received textures values to the memory. (*See* Section VIII.C.1(d), *supra.*).

Accordingly, Complainants have failed to prove by a preponderance of evidence that the '103 Accused Products meet this claim limitation recited in claim 1 of the '133 patent.

f) "an output interface configured to send said resultant value to a frame buffer"

For the reasons described above in Sections VIII.C.1(b) and (c), the SoCs containing an [redacted] do not meet this limitation, as the alleged "shading processing mechanism" does not receive a "packet," and does not produce a "resultant value from said packet." Thus, the alleged "output interface" cannot be "configured to send said resultant value to a frame buffer."

Accordingly, Complainants have failed to prove by a preponderance of evidence that the '133 Accused Products meet this limitation recited in claim 1 of the '133 patent.

Because Complainants failed to prove that the [redacted] in the '103 Accused Products involves the claimed "packet," and an ALU/memory pair and an ALU that can issue a texture request to a texture unit, the '103 Accused Products do infringe claim 1 of the '133 patent.

2. Claim 3 of the '133 Patent

a) "The shader of claim 1 wherein said output interface sends said value to said frame buffer using a valid-ready protocol."

For the reasons stated above in the discussion of claim 1, claim 1 is not infringed. Since claim 3 depends from claim 1, claim 3 is not infringed. *See Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328-29 n.5 (July 14, 2008) ("A conclusion of noninfringement as to the independent claims requires a conclusion of noninfringement as to the dependent claims."); *Monsanto Co. v. Syngenta Seeds, Inc.*, 503 F.3d 1352, 1359 (Oct. 4, 2007) ("One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim."); *Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1553 (Mar. 20, 1989) ("It is axiomatic that dependent claims cannot be found infringed unless the claims from which they depend have been found to have been infringed.").

D. Validity

1. Legal Standard: Anticipation

A determination that a patent is invalid as being anticipated under 35 U.S.C. § 102 requires a finding, based upon clear and convincing evidence, that each and every limitation is found either expressly or inherently in a single prior art reference. *See, e.g.*, *Celeritas Techs. Inc. v. Rockwell Int'l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998). Anticipation is a question of fact, including whether a limitation, or element, is inherent in the prior art. *In re Gleave*, 560 F.3d 1331, 1334-35 (Fed. Cir. 2009). The limitations must be arranged or combined the same way as in the claimed invention, although an identity of terminology is not required. *Id.* at 1334 (noting that "the reference need not satisfy an *ipsissimis verbis* test"); MPEP § 2131.

In addition, the prior art reference's disclosure must enable one of ordinary skill in the art to practice the claimed invention "without undue experimentation." *Gleave*, 560 F.3d at 1334-35. A prior art reference that allegedly anticipates the claims of a patent is presumed enabled; however, a patentee may present evidence of nonenablement to overcome this presumption. *Impax Labs., Inc. v. Aventis Pharms. Inc.*, 468 F.3d 1366, 1382 (Fed. Cir. 2006). "[W]hether a prior art reference is enabling is a question of law based upon underlying factual findings." *Gleave*, 560 F.3d at 1335.

2. None of the Asserted Claims of the '133 Patent Are Invalid as Anticipated

a) Claim 1 Is Not Anticipated by Rich (RX-0486)

U.S. Patent No. 6,108,460 issued on August 22, 2000, to Henry H. Rich ("Rich"), from U.S. Patent Application Serial No. 08/661,028 ("the '028 application") filed on June 10, 1996. (RX-0486.). The '028 application claims priority to U.S. Provisional Application Serial No. 60/032,799, which was originally filed on January 2, 1996 as U.S. Patent Application Serial No.

08/582,085. (*Id.* at 1:4-9.). There is no evidence that Rich was considered by the PTO during the prosecution of the '133 patent. (*See* JX-0003.). There is also no dispute that Rich is prior art to the '133 patent. (CPBr. at 84-87.).

Respondents alleged that Rich anticipates independent claim 1 of the '133 patent. (RBr. at 81.). Specifically, Respondents argued that Rich discloses a "unified shader" having "at least one ALU/memory pair operative to perform both texture operations and color operations." (RBr. at 78 (citing Tr. (Edwards) at 942:7–955:16, 1084:2–1152:14).).

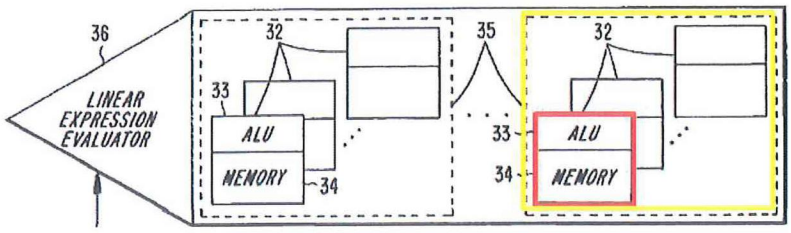
The crux of the dispute between the Parties is whether Rich discloses: (i) the claimed "unified shader"; (ii) "an input interface for receiving a packet from a rasterizer"; (iii) "texture operations compris[ing] at least one of: issuing a texture request to a texture unit and writing received texture values to the memory"; and (iv) "at least one ALU is operative to read from and write to the memory to perform both texture and color operations." (CRBr. at 43.). For the reasons discussed below, Respondents failed to demonstrate that Rich clearly and convincingly discloses these claim limitations.

Rich is directed to a system for reducing bottlenecks during computational tasking that occurs when a graphics pipeline in a GPU is generating a graphics image for display. (RX-0486 at 3:65-67.). The system disclosed in Rich involves a plurality of parallel processing elements and groups arrays of processing elements together so that they may share computing and data storage resources during computational tasking. (*Id.* at 4:3-16.). Such load sharing reduces the potential for, and degree of, computational bottlenecking. (*Id.* at 4:15-16.). This system carries out four (4) functions to convert data into an image that is output to a frame buffer: (i) geometric processing, (ii) rasterization, (iii) shading/texturing, and (iv) composition. (*Id.* at 9:53-56.).

Dr. Edwards, Respondents' invalidity expert, testified that: (i) multiple panels **35** (in

yellow below) and processing elements **32** (in red below) disclosed in Rich correspond to the claimed "unified shader"; and (ii) each processing element **32** contains an ALU **33** paired with memory **34**. (Tr. (Edwards) at 1086:22–1088:14; RX-0486 at Fig. 2.).

Figure No. 30: Figure 2 of Rich Depicting Multiple Panels and Processing Elements



(RX-0486 at Fig. 2 (annotated).).

Despite his testimony on direct, Dr. Edwards acknowledged on cross-examination that Rich does not disclose "texture coordinate shading," as required by the adopted construction of a "unified shader."

> Q: . . . The words "texture coordinate shading" don't appear anywhere in the quotes that you're relying on for texture coordinate shading, do they?
>
> A: Oh, the phrase "texture coordinate shading," no, does not appear in Rich.
>
> Q: So it's not explicitly -- texture coordinate shading is not explicitly mentioned in those quotes; correct?
>
> A: Those three words do not appear in that order.

(Tr. (Edwards) at 1196:15-24; *see also* Tr. (Wolfe) at 1390:22-25 ("[Rich] doesn't describe anything in its system as modifying or changing coordinates."); *see also id.* at 1388:18-23, 1403:7-13.).

Respondents represented that "Rich expressly discloses that Processing Element 32 within Panel 35 can ***modify*** '[t]exture u, v values' (i.e., texture coordinates)." (RBr. at 83 (emphasis added) (citing RX-0486 at 10:66–11:16).). As Complainants pointed out, Rich makes no such disclosure in the cited language or otherwise. Rather, the cited passage states that

"[t]exture u, v values are then ***generated*** by the processing elements 32." (RX-0486 at 11:5-7 (emphasis added); CRBr. at 46.).

Experts for both Complainants and Respondents agreed that the mere generation of texture coordinates is not texture coordinate shading. (Tr. (Edwards) at 1221:8–1224:11 (describing a texture mapping process—which includes generating perspective correct texture coordinates—as not involving "texture coordinate shading"); Tr. (Wolfe) at 1378:8-24, 1450:20-21.). As Respondents' expert, Dr. Edwards, confirmed, texture coordinate generation simply creates texture coordinates in the first instance. (Tr. (Edwards) at 1220:22–1224:24.). Additionally, both Dr. Edwards and Dr. Wolfe confirmed that texture coordinate cannot be ***shaded*** unless it exists, and it does not exist until it is generated (i.e., rasterized and associated with a pixel). (Tr. (Edwards) at 1220:22–1223:6, 1224:9–1225:20; Tr. (Wolfe) at 1377:14–1378:7, 1390:4-17.).

This is consistent with the '133 patent and the adopted construction of "unified shader," both of which distinguish between texture coordinate generating (a function of the rasterizer) and texture coordinate shading (a function of the unified shader). (*Markman* Order Tr. at 13:21-24; JX-0003 at 4:67–5:2 ("Unified shader **100** performs per-pixel shading calculations on rasterized values that are passed from a rasterizer unit **110**."), 5:11-14 ("rasterizer **200** generates a texture address (tc)"); *see also* Tr. (Reinman) at 172:15–174:7 ("We've got rasterization is [sic] the first step, and it's still generating texture coordinates for those incoming pixels. . . . But now that we have those texture coordinates per pixel, we can then go into texture coordinate shading at the unified shader and we can refine them, modify them."); CDX-0100.15, 16.).

Respondents also contended that processing elements **32** perform texture coordinate shading because they "perspective correct" texture coordinates. (RBr. at 83.). This is contrary to

Dr. Wolfe's testimony on direct, and Dr. Edwards' testimony on cross-examination, that perspective correction is one of the operations that a rasterizer would do when ***generating*** texture coordinates in the first instance, ***before*** texture coordinate shading can take place. (Tr. (Wolfe) at 1381:4-9, 1383:8–1384:2; Tr. (Edwards) at 1222:14-17, 1224:9–1225:20.).

> Judge McNamara: Okay. I have one question, then, before you go, Dr. Wolfe. Earlier in your testimony today, you were talking about the '133 patent, figure 2, and there was a term you used, and I quoted, and you mentioned this twice, the generated coordinates are perspective corrected.
>
> A: Yes.
>
> Judge McNamara: What does that mean?
>
> A: So when I look at this board here, I see it in perspective. It looks to me like it's getting smaller as it gets further away. ***So part of the ordinary generation of texture coordinates is that you incorporate that in your generation equation. When you generate them, if they're far away, you make them appear smaller. And that's what we call perspective correction.***

(Tr. (Wolfe) at 1458:15–1459:6 (emphasis added).

Additionally, Respondents asserted that "converting texture coordinates to 'MAP addresses' (i.e., texture addresses)" is texture coordinate shading. (RBr. 83-84.). Respondents' assertion is refuted by testimony from their own expert, Dr. Edwards, who testified that determining the texture address (the location in memory that stores color information associated with a texture coordinate) associated with a texture coordinate (the location of that same color information in the texture map) is part of the normal texture fetch process and does not involve modifying/shading the texture coordinate.

> Q: The texture coordinate is pointing to a place in the map itself, the longitude/latitude?
>
> A: That's correct.
>
> Q: To get the actual information, you need to be able to go where in the memory that longitude and latitude information was actually stored; right?

A: Yes. You need to have the texture coordinates in a form where you can use that to figure out where physically in the memory it is.

Q: ***And to do that, you use the texture coordinate and you get its pertinent texture address; right? There's a corresponding texture address that says [where for] that texture coordinate you should go in the memory and get that texel data; correct?***

A: ***Well, I think of coordinates and addresses being essentially synonymous. And I understand that AMD has that position as well.***

Q: Well, they're a little different, but they're synonymous in that they're pointing to the same area in the same information, it's just that one is in the map and one is in the memory; correct?

A: They're just different numbers to refer the same place in the map.

Q: Same place in the map; right?

A: Yes.

Q: Okay. ***None of that involved texture coordinate shading; correct?***

A: ***Not necessarily.***

Q: Your version yesterday to get the smooth map is what we just described, and you said that wasn't texture coordinate shading; correct?

A: ***Texture coordinate shading was not required to do that.***

(Tr. (Edwards) at 1223:9–1224:16 (emphases added).).

Thus, Rich does not disclose the "unified shader" required in claim 1.

Respondents also asserted that Rich expressly discloses "an input interface for receiving a packet from a rasterizer." (RBr. at 84.). Dr. Edwards opined that a separate panel **35** of the plurality of panels **35** (i.e., not the panel **35** that is operating as the claimed "unified shader") may function as a "rasterizer" because processing elements **32** in panel **35** are capable of rasterizing data to generate "contributions" (also referred to as "primitive contributions" and "primitives"). (Tr. (Edwards) at 1096:14–1099:10.). Dr. Edwards explained that the contributions generated by panel **35** contain "information associated with a pixel which allows

for the determination of a contribution value" and that this "information" includes texture coordinates and color values. (RX-0486 at 10:54-65; Tr. (Edwards) at 1097:16–1110:16.).

However, as Dr. Wolfe noted, the disclosed "contribution" does not meet the adopted construction of "packet." (Tr. (Wolfe) at 1398:1-19.). As an initial matter, the passage on which Respondents relied does not mention texture coordinate information. Rather, it only describes that each primitive contribution includes general information associated with a single pixel.

> As used herein, ***the term contributions refers to information associated with a pixel which allows for the determination of a contribution value.*** A final pixel value is then created by a combination of contribution values associated with a given pixel. The remaining primitive contributions are then optionally scattered through the processing element array **30** so that each processing element **32** only handles one contribution as seen in block **61**. When each processing element **32** of the processing element array **30** has been assigned a contribution, then the shading/texturing function is performed as reflected in block **63**.

(RX-0486 at 10:54-65 (emphasis added).). As Dr. Wolfe explained, "what's been identified by Dr. Edwards is that there is a communication, that's described in box **61** in the flowchart of Rich, in which information about pixels is sent from one processing element **32** to another. And that information about pixels does not match the Court's construction of packet . . . ." (Tr. (Wolfe) at 1397:24–1398:19.).

Moreover, the primitive contributions identified by Dr. Edwards cannot include texture coordinate information, as Respondents argued, because the texture coordinates are not generated until ***after*** the primitives are distributed. (Tr. (Wolfe) at 1398:14-16 ("[W]hat's [sent] in block **61** does not contain texture coordinates. Those are generated later."). Furthermore, Dr. Wolfe explained that until the primitives are distributed, there is no generation of texture coordinates.

> Q: And so, Jim, can you pull up column 10, lines 66 through column 11, lines 16 [of Rich]. What's described here, Dr. Wolfe?

> A: What this says is that block 71, which is shown in Figure 5, ***the u, v values for a texture lookup are generated for the first time. And this happens after the alleged packets have been distributed.*** And it's the only discussion of u, v values. The only reasonable way to read this is there are no u, v values in the contributions, and ***they are generated, in box 71 after the packets arrive at the processing elements.***

(Tr. (Wolfe) at 1401:4-14 (emphases added) (citing RX-0486 at 10:66–11:16); *see also* Tr. (Edwards) at 1204:23–1206:3; Tr. (Wolfe) at 1397:24–1398:19, 1400:12–1402:3.).

This is consistent with the disclosure in Rich, which specifies that the texture coordinates are not generated until step **71**, after the primitives are distributed in step **61**.

> The remaining primitive contributions are then optionally scattered through the processing element array **30** so that each processing element **32** only handles one contribution as seen in block **61**. When each processing element **32** of the processing element array **30** has been assigned a contribution, then the shading/texturing function is performed as reflected in block **63**.
>
> FIG. 5 illustrates the shading/texturing and composition functions of the image generation system. ***Once each processing element 32 has been assigned a contribution as seen in block 63*** then, for each assigned contribution each processing element **32** optionally calculates one or all of lighting, fog and smooth shading values as seen in block **71**. ***Texture u, v values are then generated by the processing elements 32 and perspective corrected if required as shown in block 71.***

(RX-0486 at 10:58–11:7 (emphases added), Figs. 4 and 5.).

Thus, Rich fails to disclose "an input interface for receiving a packet from a rasterizer," as required by claim 1.

Furthermore, Dr. Edwards opined that processing elements **32** request texture map data and thus "issu[e] a texture request to a texture unit." (Tr. 1107:25–1109:25.). He relied, *inter alia*, upon the following two (2) passages in Rich: (i) "[t]exture texels are then looked up by reading the texture maps from memory through the memory interface **44**"; and (ii) "256 PEs [processing elements] **32** are requesting texture map data." (*Id.*; RX-0486, 11:5-12, 22:19-36.). However, Dr. Edwards did not identify a texture module, much less one that receives the

necessary texture request from processing elements **32**.

Dr. Edwards also testified that processing elements **32** write to memory **34** the texture values that they receive as a result of sending texture requests. (Tr. (Edwards) at 1108:17-22.). However, the two (2) passages to which Dr. Edwards referred do not clearly describe such an action.

> Next, in block **120**, the block of texel data is transmitted to each processing element. Preferably, this is done by broadcasting the block address, followed by a timing code, and then, the individual texel data elements in a predetermined order indicated by the timing code. Each processing element can select, in block **121**, the texel data it needs from the stream of broadcast data. After each block is broadcast, a test is performed in block **122** to determine whether more blocks remain to be retrieved for the current list. If there are more blocks to be retrieved, control is returned to block **118**. If there are no more blocks, computation of the pixel data proceeds in block **123**. Pixel colors and intensities are computed in block **123** using standard techniques. The color component for a pixel is found by tri-linear interpolation from the corresponding color components of the eight nearest texel values.
>
> * * *
>
> With respect to the computation of pixel data in block **123** of FIG. 10, note that the full texel address stored in a PE 32 is a fractional address, which can be converted to a block address for a texel block, plus offset information. The block address designates an 8 by 8 block in texture space.

(RX-0486 at 22:27-42, 28:1-5.).

As Dr. Wolfe testified, there is no disclosure in any of these passages, or anywhere in Rich, that indicates that the texture values that processing elements **32** receive as a result of the texture request are stored in memory **34**. (Tr. (Wolfe) at 1395:8–1396:5.). He also provided persuasive testimony that Rich does not describe to where the texture data might be written.

> Q: . . . What does Rich disclose about where the ALU writes texture data to?
>
> A: Well, ***it doesn't disclose anything about where it writes texture data to. If we look at the figure in Rich, we can see that there are lots of different places in which the ALU can read results from or can write results to.*** And Dr. Edwards has identified the [ALU/memory pair] memory as memory 34, right. And there's

> no disclosure that texture data is read from memory 34 or that color data is read from memory 34 or that texture data is written to memory 34 or that color data is written to memory 34. The discussion of memory 34 occurs mostly in other parts of the disclosure, where it talks about geometry data being written there or mask data being written there. But certainly not texture data.
>
> * * *
>
> Q: Now if the ALU needs to read in information from somewhere, is the only source that it can use memory 34?
>
> A: No, ***it's got an M register that it can use and it's got some scratch pad registers that it can use, or it can just directly use the data as it comes through the M register. There's no reason for it to write it to memory. If it's waiting for this texture data, it just uses it right away. It doesn't write it to memory and save it for later.***

(Tr. (Wolfe) at 1395:8-1396:19 (emphases added).).

Dr. Edwards' testimony, including his opinion, has been given little weight.

For the foregoing reasons, Respondents have failed to prove by clear and convincing evidence that Rich anticipates claim 1 of the '133 patent.

b) Claims 1 and 3 Are Not Anticipated by Poulton (RX-0146)

U.S. Patent No. 5,481,669 issued on January 2, 1996, to John W. Poulton and others ("Poulton"), from U.S. Patent Application Serial No. 08/383,969 ("the '969 application") filed on February 6, 1995. (RX-0146.). The '969 application is a continuation of U.S. Patent Application Serial No. 07/975,821 filed on November 13, 1992, which issued as U.S. Patent No. 5,388,206. (*Id.*). There is no evidence that Poulton was considered by the PTO during the prosecution of the '133 patent. (*See* JX-0003.). There is no dispute that Poulton is prior art to the '133 patent. (CPBr. at 81-84.).

i. Claim 1

Respondents alleged that Poulton anticipates independent claim 1 of the '133 patent. (RBr. at 81.). Specifically, Respondents argued that Poulton discloses a "unified shader" having

"at least one ALU/memory pair operative to perform both texture operations and color operations." (RBr. at 78 (citing Tr. (Edwards) at 942:7–955:16, 1084:2–1152:14).).

The main dispute between the Parties is whether Poulton discloses: (i) the claimed "unified shader"; and (ii) an "ALU that performs color and texture operations by reading and writing from its memory." For the reasons discussed below, Respondents failed demonstrate that Poulton clearly and convincingly discloses these claim limitations.

Poulton is directed to a system for generating graphics images using a scalable system of circuits arrayed in parallel to compute pixel color values for primitives that, when combined, comprise the image to be displayed on screen. (RX-0146 at Abstract, 2:1-4, 3:38-61.).

> [A]t its highest level the image generation system of the present invention is comprised of a plurality of renderers **10** acting in parallel to produce a final image. The renderers **10** receive primitives of a screen image from a host processor **20** over a host interface **25**. Pixel values are then determined by the renderers **10** and the visibility of a particular pixel calculated by a given renderer determined through a compositing process and stored in the frame buffer **30** for display on the video display **40**. The linear array of renderers results in the final image being produced at the output of the last renderer.

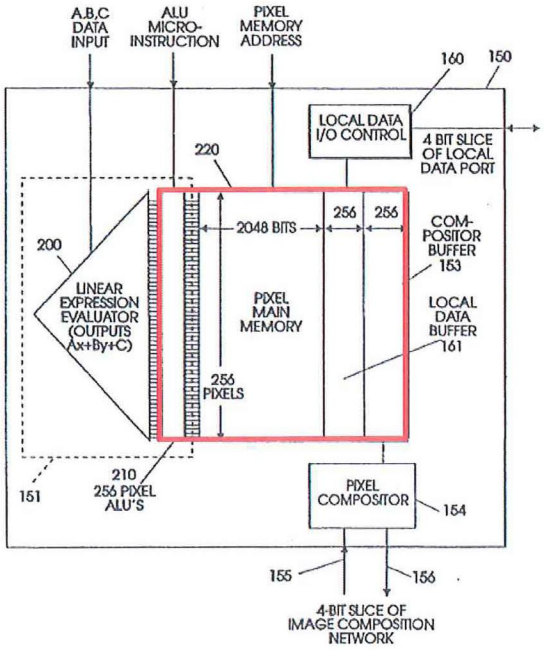
(*Id.* at 3:39-49.).

The image generation system disclosed in Poulton includes shaders, which are renderers that have a slight enhancement made to the renderer's compositor circuitry. (*Id.* at 5:28-32.). These shaders can be augmented with additional hardware to allow them to compute image-based textures in addition to procedural textures. (*Id.* at 5:32-35.).

Dr. Edwards testified that shader **15** is "a single shader circuit capable of performing color shading and texture coordinate shading." (Tr. (Edwards) at 1122:3-20.). Dr. Edwards also identified an ALU **210**/Memory **220/161/153** pair (in red below) contained in shader **15** as the claimed "ALU/memory pair," and testified that ALU **210** reads from and writes to Memory

220/161/153 to perform texture and color operations. (Tr. (Edwards) at 1136:3–1139:7, 1148:7-10.).

Figure No. 31: Figure 5 of Poulton Depicting an "ALU/Memory Pair"



(RX-0146 at Fig. 5 (annotated).).

Complainants did not dispute that shaders **15** are capable of performing color shading. (Tr. (Wolfe) at 1406:3-5; *see also* SPBr. at 51.). Rather, Complainants' expert, Dr. Wolfe opined that Poulton does not disclose texture coordinate shading. (Tr. (Wolfe) at 1406:24–1407:17 ("Q: Does Poulton disclose performing texture coordinate shading? A: It does not. It never discloses modifying a texture coordinate. It discloses ordinary texture coordinate generation in a rasterizer, and it discloses ordinary texture lookups, texture blending, but never texture coordinate shading.").). On cross, Respondents' expert, Dr. Edwards conceded the same.

> Q: All right. Slide 135 of RDX-0003C depicts what you say are passages that support a conclusion that shader 15 can do texture coordinate shading; is that correct?

A: That's correct.

Q: We'll start off small. The phrase "texture coordinate shading" doesn't appear in any of those passages, does it?

A: Not those three words.

* * *

Q: Does it explicitly describe it as capable of performing texture coordinate shading? It does not, does it?

A: Those three words do not appear.

(Tr. (Edwards) at 1236:3-10, 1239:3-6.).

Dr. Edwards relied on passages in Poulton that describe "textures," "texturing" and "texture coordinates." (Tr. (Edwards) at 1124:15–1127:14; RX-0146 at 4:10-13 ("the image generation system may further include shaders **15** which provide for ***texturing*** and shading of the image after composition by the renderers **10** and before storage in the frame buffer **30**"), 4:19-24 ("[r]egions of pixels, containing attributes such as . . . surface normal, and ***texture coordinates*** are rasterized . . . and loaded into the shaders **15**"), 5:32-34 ("[s]haders can be augmented with additional hardware to allow them to compute image-based ***textures*** in addition to procedural ***textures***"), 7:12-114 ("[s]haders **15**, which are one-board graphics computers capable of computing shading models for pixels in parallel and ***texturing***") (emphases added)).).

As Dr. Wolfe pointed out, none of these passages discuss texture coordinate shading. Respondents seem to imply that merely providing a texture coordinate to the shader **15** means that the ALU **210** within the shader **15** must necessarily have access to the texture coordinate, and be capable of performing texture coordinate shading. (Tr. (Edwards) at 1124:15–1127:14.). Evidence presented in this Investigation reflects the contrary. Poulton explicitly states that shader **15** cannot perform any texture operation unless it is further modified or "augmented."

(RX-0146 at 5:32-34 ("Shaders can be ***augmented*** with additional hardware ***to allow them to compute image-based textures*** in addition to procedural textures.") (emphases added). As Complainants noted, Poulton permits the end-user to decide whether to add additional texturing circuitry, depending on the end-user's needs. (*Id.*).

Moreover, Dr. Wolfe explained that the only augmentation of shader **15** that Poulton discloses relates to ordinary texture generation and lookups, or providing the texture coordinate to one of the internal ALUs that exist in the base configuration of shader **15**, and not the more advanced texture coordinate shading.

> Q: Does Poulton disclose performing texture coordinate shading?
>
> A: It does not. It never discloses modifying a texture coordinate. ***It discloses ordinary texture coordinate generation in a rasterizer, and it discloses ordinary texture lookups, texture blending, but never texture coordinate shading.***

(Tr. (Wolfe) at 1406:24–1407:10 (emphasis added) (citing to RX-0146 at Abstract, 4:30-34, 5:32-35, 7:12-14).).

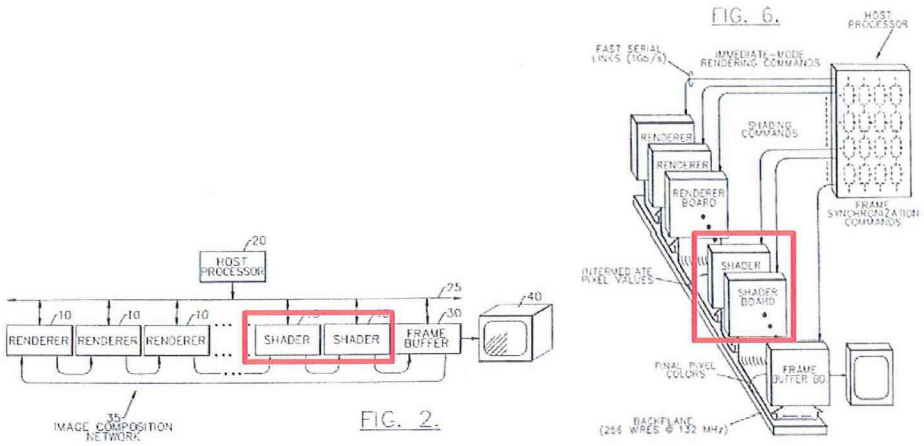
Thus, Poulton does not disclose a "unified shader" that is capable of performing texture coordinate shading.

In addition to the texture coordinate shading requirement, the claimed "unified shader" must be capable of performing color shading and texture coordinate shading within a "***single*** shader circuit." (*Markman* Order Tr. at 12:13–13:24.). Dr. Edwards opined that shader **15** is a "single shader circuit" because it includes a 128x128 pixel SIMD (single instruction multiple data) array of 64 EMCs that "collectively work together to do all the shading operations." (Tr. (Edwards) 1122:16-25; *see* RX-0146 at 13:56-59, 6:34-38 (EMCs "may be fabricated on a single integrated circuit").).

Even assuming, *arguendo*, that each shader **15** is a single circuit, Poulton explicitly

prescribes using separate shaders **15** for color and texture shading rather than a single shader **15**. Poulton illustrates and describes the use of multiple shaders 15 (in red below), such as those illustrated in Figures 2 and 6 of Poulton (reproduced in Figure No. 32 below).

Figure No. 32: Figures 2 and 6 of Poulton Showing Multiple Shaders



(RX-0146 at Figs. 2, 6 (annotated).).

Poulton also expressly states that any texture shading algorithms are performed on "separate" shaders later in the pipeline. (RX-0146 at 4:10-20 ("As shown in FIG. 2, the image generation system may further include shaders **15** which provide for texturing and shading of the image after composition by the renders **10** and before storage in the frame buffer **30**. . . . Deferred shading algorithms, such as Phong shading and procedural and ***image-based textures, are implemented on separate hardware shaders 15 that reside just ahead of the frame buffer 30***.") (emphasis added).).

Additionally, Respondents did not identify any passage in Poulton discussing shader **15** as a single circuit that performs ***both*** color and texture shading. Instead, Respondents pointed to disclosure in Poulton suggesting that some discrete parts (EMC's) of shader **15** may be

fabricated as a single circuit. Complainants' expert, Dr. Wolfe, provided persuasive testimony that each shader **15** is not a single circuit as Respondents alleged, but comprises numerous different and separate circuits.

> Q: . . . [A]re the shader boards 15 single circuits?
>
> A: No, no. ***A shader board has hundreds of chips on it, it has 64 EMC chips for doing color, then separately it's got another optional set of chips that are separately controlled. There are 32 texture ASIC chips that handle texturing. They are then connected to a whole bunch of texture memories. They're separate circuits.***
>
> Q: Do the different groups of components on shader board 15 operate as a single circuit?
>
> A: They don't. ***They have separate functions. They don't share any computational resources for different data types, and they're separately controlled.***

(Tr. (Wolfe) at 1406:6-19 (emphases added); *see also id.* at 1407:11-17.).

Moreover, Dr. Edwards' testimony to the contrary is given limited weight because he did not correctly apply the definition of unified shader when reaching his conclusions. (Tr. (Edwards) at 1280:11-22 (acknowledging that he does not understand the construction of "unified shader" to require that all elements involved in texture coordinate shading to also be involved in color shading); *see also* Section VII.E.2(a), *supra.*).

Therefore, Poulton does not disclose a single circuit that performs ***both*** color and texture shading.

Respondents contended that ALU **210**/Memory **220/161/153** pairs perform "color operations and texture operations" and that ALU **210** can read from and write to local memory (i.e., Memory **220/161/153**) to perform these operations. (RBr. at 101; Tr. (Edwards) at 1145:13-17; RX-0146 at 14:1-7, 6:44-47.). However, the passages from Poulton on which Respondents relied fail to credibly disclose the required operations.

For example, Respondents stated, "[t]o perform these operations, ALU **210** 'performs arithmetic and logical operations on the segment of local memory **220**,'" and then cited to Poulton at 6:44-47. (*Id.* at 101 (citing RX-0146 at 6:44-47 ("Each pixel processor **151** also has a small local ALU **210** that performs arithmetic and logical operations on the segment of local memory **220** which acts as the storage means **152** associated with that pixel processor and on the local value of the bilinear expression.")).). That passage makes no mention of color or texture operations, or that ALU **210** performs such operations by reading from and writing to the memory. (RX-0146 at 6:44-47.).

Respondents also identified passages in Poulton to support the assertion that ALU **210** reads from Memory **220/161/153** when issuing a texture request. (RBr. at 102 (citing RX-0146 at 6:44-48, 14:1-7 ("Each ALU **210** is a general-purpose 8-bit processor; it includes an enable register which allows operations to be performed on a subset of the pixels. The pixel ALU can use linear expression evaluator results or local memory **220** as operands and can write results back to local memory. It can also transfer data between memory and the local and compositor buffers."), Figs. 4b, 5).). However, none of the passages mention or discuss texture requests.

Additionally, Respondents claimed that "Poulton expressly discloses that ALU 210 writes received values to Memory 220/161/153," quoting Poulton at 14:32-36. (RBr. at 102 (quoting RX-0146 at 14:32-36 ("The image-composition port and local port allow pixel data to be transferred serially to/from the enhanced memory devices to other enhanced memory devices (for compositing) or to/from the texture ASICs (to perform texture lookups or pixel-data writes to texture or video memory")).). The cited passage does not mention or discuss writing received values or ALU **210**/Memory **220/161/153** pairs. (RX-0146 at 14:32-36.).

Accordingly, for the foregoing reasons, Respondents have failed to prove by clear and

convincing evidence that Poulton anticipates claim 1 of the '133 patent.

ii. Claim 3

For the reasons stated above in the discussion of claim 1, Poulton does not anticipate claim 1. Since claim 3 depends from claim 1, Poulton also does not anticipate claim 3. *See Certain Static Random Access Memories and Prods. Containing Same*, Inv. No. 337-TA-792, 2013 WL 1154018, at *10 (U.S.I.T.C. Feb. 25, 2013) (holding that because the independent claim was not anticipated, claims depending from the independent claim were also not anticipated) (citing *Hartness Int'l, Inc. v. Simplimatic Eng'g Co.*, 819 F.2d 1100, 1108 (Fed. Cir. 1987).).

3. Claim 3 of the '133 Patent Is Not Obvious Over Rich (RX-0486) in Combination with Poulton (RX-0146)

Respondents contended that Rich in view of Poulton renders claim 3 of the '133 patent obvious. (RBr. at 104 (citing Tr. (Edwards) at 1116:25–1121:2).). Dr. Edwards opined that it would be obvious to a person of ordinary skill in the art to utilize the valid-ready protocol disclosed in Poulton with the output interface and frame buffer in Rich. (Tr. (Edwards) at 1116:25–1121:2).). Respondents' allegations and Dr. Edwards' testimony fail for the following reasons.

Respondents' obviousness defense relies on Poulton only for its disclosure of a valid-ready protocol. (RBr. at 104.). However, as discussed in Section VIII.D.2(a) above, Rich does not clearly and convincingly disclose the claimed "unified shader," "an input interface for receiving a packet from a rasterizer," "texture operations compris[ing] at least one of: issuing a texture request to a texture unit and writing received texture values to the memory," and "at least one ALU is operative to read from and write to the memory to perform both texture and color

operations" required by claim 1 and its dependent claim 3. Thus, Respondents' obviousness defense fails for the same reasons as their anticipation defense against claim 1, discussed in Section VIII.D.2(a) above.

Moreover, Respondents did not provide any evidence that one of ordinary one of ordinary skill would have been motivated to combine Rich with Poulton to produce the GPU recited in claim 3 of the '133 Patent. (Tr. (Wolfe) at 1403:25–1405:13.). Respondents simply asserted generally that the valid-ready protocol was basic and well-known, without identifying any reason why one would modify the Rich system to include a valid-ready protocol. (RBr. at 104-05.). Complainants' expert, Dr. Wolfe, presented unrebutted testimony that because of Rich's unique architecture, there is no motivation to combine.

> Q: Would it make sense to borrow the valid-ready protocol of Poulton and use it for Rich?
>
> A: It doesn't. Poulton does disclose a valid-ready protocol, but the valid-ready protocol is -- the valid-ready protocol makes sense when you have a configuration like Poulton. And it's very much like the way Dr. Edwards described it. If I were calling the Judge on the phone and we wanted to decide who was going to speak, we might use a protocol like that. ***But that scenario doesn't come up in Rich. Rich instead has a big shared bus with dozens or hundreds of units all sharing it, and some of them are isolated at different times, some of them are connected at different times. And there's no way for valid-ready protocol to work. So instead, Rich has -- I don't know if they call it central bus controller or global bus controller, I think they call it a global bus controller, that's part of central controller 38 that controls the whole thing from one location.*** That's what makes sense in Rich, not the valid-ready protocol.

(Tr. (Wolfe) at 1403:25–1405:6 (emphasis added).

For the foregoing reasons, Respondents have failed to prove by clear and convincing evidence that claim 3 of the '133 is rendered invalid as obvious by Rich in view of Poulton.[46]

[46] Complainants did not identify any evidence of secondary considerations in their pre- and post-hearing

IX. DOMESTIC INDUSTRY REQUIREMENT: TECHNICAL PRONG

A. Complainants Have Satisfied the Technical Prong of the Domestic Industry Requirement

1. '506 Patent

The private parties stipulated that the technical prong of the domestic industry requirement is satisfied for the '506 patent. (Doc. ID No. 626915 (DI Stipulation) (Oct. 27, 2017).). In addition, Complainants' expert, Dr. Reinman, testified as to how each limitation of claims 1-5 and 8 of the '506 patent is satisfied in the DI Multi Shader Products. (Tr. (Reinman) at 309:18–323:6, 341:14–363:1.). The undisputed evidence therefore demonstrates that Complainants' DI Multi Shader Products practice claims of the '506 patent as indicated below, and that Complainants have met the technical prong of the domestic industry requirement.

AMD Product	'506 Patent Claims Practiced
Bristol Ridge	1, 8, 9
Carrizo	1, 8, 9
Fiji	1-9
Iceland	1, 8, 9
Polaris 10	1-9
Polaris 11	1-9
Polaris 12	1-9
Polaris 22	1-9
Tonga	1-9
Stoney Ridge	1, 8, 9
Raven Ridge	1, 8, 9
Vega 10	1-9
Vega 12	1-9

briefing, or during the evidentiary hearing.

AMD Product	'506 Patent Claims Practiced
Vega 20	1-9

(DI Stip. at ¶¶ 2, 4, 6-7.).

2. '133 Patent

The private parties stipulated that the technical prong of the domestic industry requirement is satisfied for the '133 patent. (DI Stip.). In addition, Complainants' expert, Dr. Reinman, testified as to how each limitation of claims 1, 3 and 8 of the '133 patent is satisfied in the DI Single Shader and Multi Shader Products. (Tr. (Reinman) at 363:2–378:4.). The unrebutted evidence therefore shows that Complainants' DI Single Shader and Multi Shader Products practice claims of the '133 patent as indicated below, and that Complainants have met the technical prong of the domestic industry requirement.

AMD Product	'133 Patent Claims Practiced
Bristol Ridge	1, 3, 8, 40
Carrizo	1, 3, 8, 40
Fiji	1, 3, 8, 40
Iceland	1, 3, 8, 40
Polaris 10	1, 3, 8, 40
Polaris 11	1, 3, 8, 40
Polaris 12	1, 3, 8, 40
Polaris 22	1, 3, 8, 40
Tonga	1, 3, 8, 40
Stoney Ridge	1, 3, 8, 40
Raven Ridge	1, 3, 8, 40
Vega 10	1, 3, 8, 40
Vega 12	1, 3, 8, 40

AMD Product	'133 Patent Claims Practiced
Vega 20	1, 3, 8, 40

(DI Stip. at ¶¶ 2, 4, 6-7; RPBr. at 74.).

X. DOMESTIC INDUSTRY REQUIREMENT: ECONOMIC PRONG

A. Complainants Have Satisfied the Economic Prong of the Domestic Industry Requirement Under Section 337(a)(A), (B), and (C)

The private parties stipulated that the economic prong of the domestic industry is satisfied. The unrebutted evidence thus shows that, as a result of Complainants' activities associated with their DI Products, Complainants have met the economic prong of the domestic industry requirement. (DI Stip. at ¶¶ 6-7; *see also* Motion Docket No. 1044-040 (Complainants' Motion for Summary Determination that the Economic Prong of the Domestic Industry Requirement Is Satisfied) at 7-21 (Sept. 28, 2017).).

XI. RECOMMENDATION ON REMEDY AND BOND

This decision recommends: (1) a limited exclusion order ("LEO") with a certification provision; (2) a cease and desist order ("CDO") against Respondents SDI and VIZIO; and (3) that no bond of be issued for the Presidential Review Period.

A. Legal Standard

Pursuant to Commission Rule 210.42, an ALJ must issue a recommended determination on: (i) an appropriate remedy if the Commission finds a violation of Section 337, and (ii) an amount, if any, of the bond to be posted. 19 C.F.R. § 210.42(a)(1)(ii). When a Section 337 violation has been found, as here, "the Commission has the authority to enter an exclusion order, a cease and desist order, or both." *Certain Flash Memory Circuits and Prods. Containing the Same*, Inv. No. 337-TA-382, Comm'n Opinion on the Issues Under Review and on Remedy, the

Public Interest and Bonding, at 26 (June 9, 1997).

Upon a finding of infringement, 19 U.S.C. § 1337(d) provides for a LEO, directed to the products of named respondents, excluding any articles that infringe one or more claims of the asserted patents. 19 U.S.C. § 1337(d). A CDO is also appropriate where the evidence demonstrates the presence of commercially significant inventory in the United States. 19 U.S.C. § 1337(f); *see also Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, Comm'n Opinion, USITC Pub. No. 2391, 1991 WL 790061 at *30-32 (June 1991). Infringing articles may enter upon the payment of a bond during the sixty-day Presidential Review Period. 19 U.S.C. § 1337(j)(3). The bond is to be set at a level sufficient to "offset any competitive advantage resulting from the unfair method of competition or unfair act enjoyed by persons benefiting from the importation." *Certain Dynamic Random Access Memories, Components Thereof and Prods. Containing Same*, Inv. No. 337- TA-242, Comm'n Opinion, 1987 WL 450856 at 37 (Sept. 21, 1987).

B. A Limited Exclusion Order with a Certification Provision Is Warranted

In the event of a finding of violation of Section 337, Complainants requested that the Commission issue a LEO, with no certification provision, barring the entry of Respondents VIZIO's, MediaTek's, and SDI's graphics systems, components thereof and consumer products containing same. (CBr. at 96-110.). Staff recommended that a LEO with a certification provision issue against Respondents VIZIO's, MediaTek's and SDI's infringing products. (SBr. at 43-48.). Respondents argued that any LEO should cover only the accused chipsets that were found to infringe one or more claims of the Asserted Patents, and should not capture "downstream products," specifically, Respondent VIZIO's televisions. (RPBr. at 89-93; RBr. at 107-21.). Respondents agreed with Staff that any LEO should include a certification provision.

(RBr. at 107.).

In this case, the Commission and the U.S. Customs and Board Protection ("CBP") should accept a LEO with a certification provision because whether a consumer product infringes the asserted patents claims is not readily apparent by inspection. *Certain Digital Televisions & Certain Prods. Containing Same & Methods of Using Same*, Inv. No. 337-TA-617, Comm'n Opinion at 11 (Apr. 23, 2009) ("Certification provisions are necessary to minimize the possibility that non-infringing products will be excluded from entry into the United States when CBP is unable to easily determine by inspection whether an imported product violates a particular exclusion order.").

C. Respondent VIZIO's Accused Products Are Not Excluded from the LEO

Relying on the Commission decision in *Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, and Processes for Making Such Memories*, Respondents contended that if a LEO is issued, the LEO should not extend to Respondent VIZIO's "downstream" television products. (RPBr. at 89-93 (citing *Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, and Processes for Making Such Memories*, Inv. No. 337-TA-276, Comm'n Opinion at 123-26, USITC Pub. No. 2196 (May 1989) ("*EPROMs*"), *aff'd sub nom., Hyundai Elec. Indus. Co., Ltd. v. United States Int'l Trade Comm'n*, 899 F.2d 1204 (Fed. Cir. 1990)); RBr. at 107-21 (citing same).).[47]

[47] While Respondents acknowledged that the Commission's opinion in *EPROMs* concerned downstream products, Respondents argued that *EPROMs* remains controlling law in the wake of *Kyocera Wireless Corp. v. International Trade Commission*, 545 F.3d 1340 (Fed. Cir. 2008). (RBr. at 110.). Respondents cited to determinations and opinions post-*Kyocera* by ALJs and the Commission weighing the nine *EPROMs* factors in investigations involving downstream products of named respondents. (*Id.* at 110-11 (citing *Certain Microprocessors, Components Thereof and Prods. Containing Same*, No. 337-TA-781,

Complainants asserted that the *EPROMs* factors have no applicability or usefulness in this Investigation because the only products they seek to exclude: (1) are those of the named Respondents, and are accused products properly within the scope of a LEO; and (2) are not "downstream products" as that term is used in the context of *EPROMs* jurisprudence. (CBr. at 98.). For the reasons discussed below, I agree with Complainants and find that the *EPROMs* factors do not apply to Respondent VIZIO's accused televisions.[48]

The *EPROMs* decision concerns the scope of the Commission's authority under 19 U.S.C. § 1337(d) to issue exclusion orders. Section 1337(d) provides, in relevant part: "If the Commission determines, as a result of an investigation under this section, that there is a violation of this section, it shall direct that the articles concerned, ***imported by any person violating the provision of this section***, be excluded from entry into the United States . . . ." 19 U.S.C. § 1337(d)(1) (emphasis added).

In *EPROMs*, complainant Intel accused specific EPROMs manufactured by respondent

---

2012 WL 6883205, at *175 (Dec. 14, 2012); *Certain Liquid Crystal Display Modules, Prods. Containing Same, and Methods Using the Same, No. 337-TA-634*, Comm'n Opinion at 4 (Nov. 24, 2009) (adopting the ALJ's analysis of the EPROMs factors); *Certain Audiovisual Components and Prods. Containing the Same*, No. 337-TA-837, 2013 WL 4408170, at *3 (July 31, 2013); *Certain Light-Emitting Diodes and Prods. Containing the Same*, No. 337-TA-784, 2012 WL 3246531, at *4 (Jul. 23, 2012). As my colleagues have acknowledged, to date, there is no clear precedent on this issue. *See, e.g., Certain Flash Memory Chips and Prods. Containing Same*, Inv. 337-TA-893, Order No. 51 at 3 (Sept. 29, 2014); *Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, Order No. 57 at 2 (Nov. 21, 2014). However, for the reasons stated, I find that an analysis of the *EPROMs* factors is not germane where, as here, the products found to infringe are manufactured and imported by a named Respondent in this Investigation. *See, e.g., Certain Static Random Access Memories and Products Containing Same*, Inv. No. 337-TA-792, Initial Determination at 62 (Dec. 12, 2012); *Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, Initial Determination at 213 (Feb. 27, 2015) (finding that the *EPROMs* factor do not apply because the accused products are not "downstream" products); *Certain Flash Memory and Prods. Containing Same*, Inv. No. 337-TA-685 (Feb. 28, 2011) (finding an *EPROMs* analysis "unnecessary" for a named respondent's own products).

[48] Staff also noted, "it is not clear whether the EPROMs factors are still applicable." (SBr. at 45.).

Hyundai of violating Section 337. *EPROMs* at 3-5. In addition to the accused EPROM products, Intel sought to exclude a broad array of other products that incorporated the accused EPROM products, but were otherwise not the subject of a finding of infringement and a Section 337 violation. *Id.* at 118 n.146. These products included computers, telecommunication equipment, automotive electronic equipment, and automobiles, that, according to Intel, "as a general rule, contain EPROMS, and ***may*** therefore in the future contain infringing EPROMs." *Id.* (emphasis added).

With regard to the ***accused*** products in that case that were specifically determined to infringe and the subject of a Section 337 violation, the Commission concluded that "[e]xclusion of the specific articles found to infringe the patents at issue in the investigation is ***obviously appropriate***. Therefore, the limited exclusion order applies to EPROMs of the specific densities (64K, 256K, 512K, and 1M) which have been determined to infringe the patents at issue." *Id.* at 121 (emphasis added).

With respect to the ***other*** products that Intel sought to exclude, i.e., products of ***non-*** respondents, the Commission explained that the factors set forth in *EPROMs* were conceived for the following specific purpose:

> [T]he Commission may, in issuing exclusion orders, whether general or limited, balance the complainant's interest in obtaining complete protection from all infringing imports by means of exclusion of downstream products against the inherent potential of even a limited exclusion order, when extended to ***downstream products***, to disrupt legitimate trade in ***products which were not themselves the subject of a finding of violation of section 337***. In performing this balancing, the Commission may consider such matters as the . . . [9 *EPROMs* factors].[49]

[49] The *EPROMs* factors, which are not exclusive, include: (1) the value of the infringing articles compared to the value of the downstream products in which they are incorporated, (2) the identity of the

Id. at 125 (emphases added).

Thus, the *EPROMs* factors devised by the Commission in its 1989 decision were intended to act as a safeguard against undue harm to importers of "downstream products," that is, "products which were not themselves the subject of a finding of violation." *Id.*

This concern has been substantially, if not entirely, obviated by the Federal Circuit's 2008 opinion in *Kyocera Wireless Corp. v. International Trade Commission*, 545 F.3d 1340 (Fed. Cir. 2008). *See, e.g., Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same*, Inv. No. 337-TA-661, Comm'n Opinion at 12 (U.S.I.T.C. July 26,2010) (issuing a limited exclusion order, which covered downstream products of named respondents, without analysis of *EPROMs* factors); *Certain Static Random Access Memories and Products Containing the Same*, Inv. No. 337-TA-792, Initial Determination at 62 (U.S.I.T.C. Oct. 25, 2012) ("*Static Random Access Memories*") (recommending the issuance of a LEO directed to downstream products without conducting an *EPROMs* analysis and citing to the Commission's opinion in Inv. No. 337-TA-661).[50]

---

manufacturer of the downstream products (i.e., whether the downstream products were manufactured by the party found to have committed the unfair act, or by third parties), (3) the incremental value to complainant of the exclusion of downstream products, (4) the incremental detriment to respondents of such exclusion, (5) the burdens imposed on third parties resulting from exclusion of downstream products, (6) the availability of alternative downstream products which do not contain the infringing articles, (7) the likelihood that imported downstream products actually contain the infringing articles and are thereby subject to exclusion, (8) the opportunity for evasion of an exclusion order which does not include downstream products, and (9) the enforceability of an order by Customs. *EPROMS* at 125.

[50] Chief ALJ Bullock found that:

> The Notice of Investigation makes clear that the Investigation concerns "certain static random access memories and products containing the same" that infringe one or more claims of the asserted patents. 76 Fed. Reg. 45,295-296 (July 28, 2011).) Thus, not only are GSI's SRAMs accused of infringement in this Investigation, but Cisco's and Avnet's products containing the accused GSI SRAMs are themselves accused of infringement in this Investigation. *See Certain Semiconductor Chips with Minimized Chip Package Size*

In *Kyocera*, the Federal Circuit held that a limited exclusion order can only be applied against "named respondents that the Commission finds in violation of Section 337." *Kyocera*, 545 F.3d at 1356. Thus, after *Kyocera*, any entity whose products may be affected by a limited exclusion order has an opportunity to be fully heard as a party to the investigation. *Id. Kyocera* therefore mitigates the due process concerns that previously existed at the time of *EPROMs*, when a limited exclusion order could be applied to "products which [are] not themselves the subject of a finding of violation," as discussed above. *See EPROMs* at 125.

The circumstances that justified the *EPROMs* balancing test in 1989 are not present in this Investigation. In contrast to the "downstream products" at issue in *EPROMs*, there are no such "downstream products" at issue here. The LEO that Complainants seek is limited to only those VIZIO products that are specifically accused in this Investigation, and are imported and sold by VIZIO, a respondent named in this Investigation. Accordingly, I find that an analysis of the *EPROMs* factors is not germane.[51]

> *& Prods. Containing Same*, Inv. No. 337-TA-605, Int: Det. at 125 (Dec. 1, 2008). Should the Commission therefore find a violation, the undersigned recommends that the Commission issue a limited exclusion order prohibiting the importation of GSI's infringing SRAM products and products containing same. *See Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Prods. Containing Same*, Inv. 337-TA-661,Comm'n Op. at 12 (July 26, 2010) (determining to issue a limited exclusion order, which covered the downstream products of the named respondents, ***without analysis of the EPROM factors.***)

Static Random Access Memories at 62 (emphasis added).

[51] In the event that the Commission disagrees and finds that an analysis of the *EPROMs* factors ("Factors") is appropriate, evidence adduced in this Investigation weighs in favor of the exclusion of the VIZIO Accused Products. Although the evidence that Respondents introduced through their remedy expert, Dr. Thomas D. Vander Veen, was not adequately rebutted, Dr. Vander Veen's opinions were based on inaccurate evidence and assumptions. For example, with regard to what he considered in his analysis of *EPROMs* Factor ***one*** (the value of the infringing articles compared to the value of the downstream products in which they are incorporated), Dr. Vander Veen acknowledged that he: (1) performed solely a quantitative analysis (Tr. (Vander Veen) at 923:6-9 ("Q: Doctor, is it your testimony

here today that you do address the qualitative benefits of the product? A: No, I don't address the qualitative benefits of the product."); (2) used inflated sales information (Tr. (Vander Veen) at 926:3-9 (admitted to including an unknown number of non-accused products in potentially affected VIZIO sales calculations; comparison of CPBr. at Appendix A and RX-0389C shows sales data included 85 non-accused products)); (3) failed to distinguish accused products from non-accused products in estimating the amount of VIZIO sales subject to the requested LEO (Tr. (Vander Veen) at 905:11-18); (4) did not include price information for eight of the eleven accused GPUs in calculating the average cost of such components (*id.* at 915:5-8, 17-21); (5) included a royalty rate calculation that was not disclosed in his expert report and was presented for the first time during the evidentiary hearing, which he admitted may not even be subject to the royalty bearing license agreement and may include GPUs for which no royalties were paid (*id.* at 916:19–919:9, 920:3-11); and (6) did not investigate and does not know whether the accused component was the highest price component in the VIZIO Accused Products (*id.* at 913:2-8). Similarly, the evidence Respondents adduced concerning royalties paid for patents that license GPU technology is problematic. The [redacted] on which Respondents relied has a [redacted] which requires [redacted] (RX-0393C (A11-[redacted] Agreement) at § 3.1, Ex. F (engineering fees and royalty rates for each tier). The effective royalty rate calculation offered by Dr. Vander Veen was based on an estimate that may have included GPUs for which [redacted]. (Tr. (Vander Veen) at 916:19–919:9 (conceding that he was not able to determine what royalty-bearing units for which royalties were paid).). For these reasons, his opinion was given little weight.

Moreover, based on evidence presented in this Investigation, at least *EPROMs* Factors ***two*** (the identity of the manufacturer of the downstream products), ***six*** (the availability of alternative downstream products that do not contain the infringing articles), ***seven*** (the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion), and ***eight*** (the opportunity for evasion of an exclusion order that does not include downstream products), weigh in favor of exclusion:

(i) Factor ***two***: Complainants are only seeking a LEO against products manufactured and sold by Respondent VIZIO. These products are branded products of Respondent VIZIO and come into the United States in conspicuously branded VIZIO packaging. (*See, e.g.*, CPX-0006; CPX-0007.).

(ii) Factor ***six***: Complainants presented evidence that their licensees [redacted] account for 13 percent and 16 percent, respectively, of the same market, and can provide alternative products that do not include the infringing SoCs. (RX-0543.0019, CX-0366.).

(iii) Factor ***seven***: All of the VIZIO Accused Products are accused products subject to exclusion. (JX-0010C, JX-0011C.).

(iv) Factor ***eight***: The only VIZIO Accused Products are televisions assembled overseas. An overwhelming majority of the Accused Products of MediaTek and SDI [redacted] (*See* CX-3848C (MediaTek Resp. to Interrog. No. 17) at 36 ([redacted]); CX-4204C (SDI Resp. to RFA No. 134) at 10 ([redacted]).). A LEO that does not include the accused VIZIO televisions would exclude an extremely small percentage of the Accused Products and render the requested relief virtually meaningless.

With regard to *EPROMs* Factors ***three*** (the incremental value to the complainant of the exclusion of downstream products), ***four*** (the incremental detriment to the respondents of such exclusion), ***five*** (the burdens imposed on third parties resulting from exclusion of downstream products), and ***nine*** (the

D. No Bond During the Presidential Review Period Is Warranted Against Respondents

Complainants have requested a recommendation that the Commission impose a bond during the Presidential Review Period of 100% of the entered value of any and all products subject to an exclusion order in this Investigation. (CBr. at 110-11.). Staff contended that unless Complainants can identify adequate record evidence that a price comparison or a reasonable royalty is not practical, in which case a 100% bond is appropriate, no bond or a minimal bond is appropriate. (SBr. at 51.). According to Respondents, Complainants failed to sustain their burden with regard to any bond and argued that no bond or a minimal bond during the Presidential Review Period is proper. (RRBr. at 73.).

The Commission frequently sets the bond based on the difference in sales prices between the patented domestic product and the infringing product. *See, e.g., Certain Microsphere Adhesives, Process for Making Same, and Prods. Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, USITC Pub. No. 3949, Comm'n Opinion at 24 (Jan. 1996). In other instances where a direct comparison between a patentee's product and the accused product is not possible, the Commission has set the bond at a reasonable royalty rate. *See, e.g., Certain Integrated Circuit Telecommunication Chips and Prods. Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm. Opinion at 41-43 (Aug. 3, 1993). Commission precedent allows for a 100 percent bond when it is not practical or possible to set the bond based on price differential. *Certain Voltage Regulators, Components Thereof and*

---

enforceability of an order by Customs), the record evidence is unclear whether these Factors weigh in favor or against the exclusion of VIZIO's television.

For the foregoing reasons, an analysis of the *EPROMs* factors supports the inclusion of Respondent VIZIO's televisions in the LEO and exclusion of the VIZIO televisions should a LEO issue.

Prods. Containing Same, Inv. No. 337-TA-564, Comm'n Opinion at 79 (Public Version Oct. 19, 2007). The purpose of the bond is to protect the complainant from any injury. 19 U.S.C. § 1337(j)(3); 19 C.F.R. §§ 210.42(a)(1)(ii), 210.50(a)(3).

Complainants bear the burden of establishing the need for a bond, including the amount of bond. *See, e.g., Certain Rubber Antidegradants, Components Thereof & Prods. Containing Same*, USITC Pub. No. 3975, Inv. No. 337-TA-533, Comm'n Opinion at 40 (April 2008); *Certain Coenzyme Q10 Products and Methods of Making Same*, Inv. No. 337-TA-790, Initial and Recommended Determination (Sept. 27, 2012) (recommending Commission not impose a bond because complainant failed in its burden to demonstrate the appropriate bond amount); *Certain Mobile Telephones and Wireless Communication Devices Featuring Digital Cameras, and Components Thereof*, Inv. No. 337-TA-703, Recommended Determination (Jan. 24, 2011) (recommending no bond because complainant did not meet its burden in providing evidence on the necessity of a bond); *Certain Liquid Crystal Display Devices and Prods. Containing the Same*, Inv. No. 337- TA-631, Comm'n Opinion at 27-28 (July 14, 2009) (setting zero bond because complainant "simply claimed that it was impossible to conduct a price differential analysis" and "should not benefit from a lack of any effort to identify" relevant pricing information, particularly that which is in its possession).

As Complainants and Staff noted, evidence presented in this Investigation indicates that the variety of products at issue here may make it difficult to calculate a price differential between the accused products and products made by Complainants and their licensees. (*See, e.g.*, CX-0316C (Dep. Tr. of Scott D. Patten[52] (July 19, 2017)) at 18:15–32:7, 25:1–27:16, 30:20–42:33,

[52] VIZIO identified Mr. Scott D. Patten as a 30(b)(6) witness. During his deposition taken on July 19,

43:14–47:14; CX-0257C (Dep. Tr. of Michael Lin[53] (June 28, 2017)) at 36:1–43:15.).

Additionally, Complainants and Staff pointed to evidence of royalties charged in [redacted], which include [redacted]. (*See, e.g.*, CX-0364C (ATI-[redacted] Agreement) at Ex. F ([redacted]); CX-0365 (First Amendment to ATI-[redacted] Agreement) at § 4 ([redacted]); Tr. (Vander Veen) at 915:22–922:2.). Thus, the royalty rate charged in these [redacted] does not appear to be an [redacted] in this Investigation.

Despite this showing, Complainants failed to meet their burden. During the evidentiary hearing, Complainants did not present any evidence demonstrating that Respondents' acts have caused Complainants competitive injury, or that a bond would be necessary during the Presidential Review Period. Specifically, Complainants' products do not [redacted]. (Tr. (Vander Veen) at 886:15-17.). Thus, a bond would not protect Complainants from competitive injury. *See, e.g.*, *Certain Semiconductor Integrated Circuits*, Inv. No. 337-TA-665, Initial Determination (issue not reached by the Commission), 2009 WL 5942422, at *281-82 (Oct. 14, 2009) (recommending that no bond be imposed on respondents, as "[e]ven when [Complainant] was manufacturing and selling products in the U.S., [its] products did not compete with Respondents' products. . . . Thus, a bond would not protect [Complainant] from competitive injury"). For the foregoing reasons, it is recommended that no bond is

---

2017, Mr. Patten provided testimony on certain topics on behalf of VIZIO. (CX-0316C at 10:20-22.).

[53] When he testified during his deposition on June 28, 2017, Mr. Michael Lin was the Vice President of Operation at Sigma Designs. (CX-0257C at 6:19–7:1.). SDI identified Mr. Lin as a 30(b)(6) witness to testify on certain topics on behalf of SDI. (*Id.* at 10:23–11:1.).

warranted during the Presidential Review Period.

E. A Cease and Desist Order Is Warranted

Complainants requested that CDOs issue against Respondents VIZIO and SDI. (CBr. at 96-110.). Staff recommended that a CDO issue against at least Respondent VIZIO in the event a violation of Section 337 is found. (SBr. at 43-48.). Respondents asserted that no CDO should be issued because Respondents do not maintain a commercially significant inventory in the United States. (RBr. at 121.).

The evidence adduced in this Investigation demonstrates that both Respondents VIZIO and SDI currently maintain commercially significant inventories of infringing products within the United States. For example, Respondent SDI disclosed in its interrogatory responses that it has a domestic inventory of [redacted]. (CX-3871C.0039.). In Respondent VIZIO's Stipulation and Agreement Regarding Importation and Inventory, Respondent VIZIO stated that it has domestic inventory of [redacted]. (JX-0010C.0025-29; *see also* CX-0316C; CX-0257C; CX-3752C; CX-3857C; CX-3863C; CX-3865C; CX-3869C; CX-3760C; CX-3873C; CX-4203C; JX-0010C.).

Because these domestic inventories are commercially significant, it is recommended that CDOs be issued against Respondents VIZIO and SDI.

XII. WAIVER OR WITHDRAWAL OF RESPONDENTS' DEFENSES

Respondents did not raise in their Pre-Hearing Brief or offer any evidence during the evidentiary hearing to support: (1) Respondent VIZIO's Sixth Affirmative Defense (lack of unfair act), Seventh's Affirmative Defense (prosecution history estoppel) and Eighth Affirmative Defense (waiver and estoppel); and (2) Respondents MediaTek's and SDI's Fourth Affirmative

Defense (license), Fifth Affirmative Defense (prosecution history estoppel/disclaimer), Sixth Affirmative Defense (substantial non-infringing uses), Seventh Affirmative Defense (unenforceability), Tenth Affirmative Defense (no unfair act), Eleventh Affirmative Defense (lack of standing) and Twelfth Affirmative Defense (other defenses).

Consequently, it is a finding of this decision that these Affirmative Defenses have been withdrawn, waived and/or abandoned consistent with Ground Rules 7.2 and 10.1. *Kinik Co. v. Int'l Trade Comm'n*, 362 F.3d 1359, 1367 (Fed. Cir. 2004).

XIII. CONCLUSIONS OF FACT OR LAW: THIS INITIAL DETERMINATION FINDS A SECTION 337 VIOLATION BASED UPON INFRINGEMENT OF U.S. PATENT NO. 7,633,506

1. The Commission has subject matter, personal, and *in rem* jurisdiction in this Investigation.

2. The Accused Products have been imported into the United States.

3. Complainants have proven by a preponderance of evidence that the Accused Multipipe Products infringe asserted claims 1-5 and 8 of U.S. Patent No. 7,633,506.

4. Complainants have not proven by a preponderance of evidence that the Accused Singlepipe and Multipipe Products infringe asserted claims 1 and 3 of U.S. Patent No. 7,796,133.

5. Respondents have not proven by clear and convincing evidence that asserted claims 1-5 and 8 of U.S. Patent No. 7,633,506 are invalid.

6. Respondents have not proven by clear and convincing evidence that asserted claims 1 and 3 of U.S. Patent No. 7,796,133 are invalid.

7. Complainants have proven that they satisfy the technical prong of the domestic industry requirement for U.S. Patent Nos. 7,633,506 and 7,796,133.

8. Complainants have proven that they satisfy the economic prong of the domestic industry requirement.

9. Complainants have proven that Respondents have violated Section 337 of the Tariff Act of 1930, as amended.

The lack of discussion of any matter raised by the Parties, or any portion of the record, does not indicate that it has not been considered. Rather, any such matter(s) or portion(s) of the record has/have been determined to be irrelevant, immaterial or meritless. Arguments made on briefs, which were otherwise unsupported by record evidence or legal precedent, have been accorded no weight.

XIV. CONCLUSION AND ORDER

Based upon the foregoing, it is my Initial Determination on Violation of Section 337 that Respondent VIZIO, Respondent MediaTek, and Respondent SDI have violated Section 337 of the Tariff Act of 1930, as amended, by importing into the United States, selling for importation, or selling within the United States after importation of certain graphic systems, components thereof, and consumer products containing the same, by reason of infringement of claims 1-5 and 8 of United States Patent No. 7,633,506.

I have found that Respondent VIZIO, Respondent MediaTek, and Respondent SDI have not violated Section 337 of the Tariff Act of 1930, as amended, by importing into the United States, selling for importation, or selling within the United States after importation of graphic systems, components thereof, and consumer products containing the same, by reason of infringement of claims 1 and 3 of United States Patent No. 7,796,133.

This Initial Determination on Violation of Section 337 of the Tariff Act of 1930 is certified to the Commission. All orders and documents, filed with the Secretary, including the exhibit lists enumerating the exhibits received into evidence in this Investigation, that are part of the record, as defined in 19 C.F.R. § 210.38(a), are not certified, since they are already in the Commission's possession in accordance with Commission Rules. *See* 19 C.F.R. § 210.38(a). In accordance with 19 C.F.R. § 210.39(c), all material found to be confidential under 19 C.F.R.

§ 210.5 is to be given *in camera* treatment.

After the Parties have provided proposed redactions of confidential business information ("CBI") that have been evaluated and accepted, the Secretary shall serve a public version of this ID upon all parties of record. The Secretary shall serve a confidential version upon counsel who are signatories to the Protective Order (Order No. 1) issued in this Investigation.

Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission unless a party files a petition for review pursuant to 19 C.F.R. § 210.43(a) or the Commission, pursuant to 19 C.F.R. § 210.44, orders on its own motion a review of the Initial Determination or certain issues therein.

Within fourteen (14) days of the date of this document, the Parties shall submit to the Office of Administrative Law Judges a joint statement regarding whether or not they seek to have any portion of this document deleted from the public version. The Parties' submission shall be made by hard copy and must include a copy of this ID with red brackets indicating any portion asserted to contain CBI to be deleted from the public version. The Parties' submission shall also include an index identifying the pages of this document where proposed redactions are located. The Parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.

MaryJoan McNamara
Administrative Law Judge

Inv. No. 337-TA-1044
App. A to ID
April 13, 2018

APPENDIX A: ACCUSED PRODUCTS[1]

1. Respondent VIZIO's Accused Products

Table No. 1: Accused VIZIO Singlepipe Products

Accused VIZIO Singlepipe Product	Integrated Circuit Supplier	Integrated Circuit Model	GPU Core	Configuration

(CPBr. at App. A.).

Table No. 2: Accused VIZIO Multipipe Products

Accused VIZIO Multipipe Product	Integrated Circuit Supplier	Integrated Circuit	GPU Core	Configuration

[1] The information contained in these tables was taken from Appendix A of Complainants' Pre-Hearing Brief.

Accused VIZIO Multipipe Product	Integrated Circuit Supplier	Integrated Circuit	GPU Core	Configuration

Accused VIZIO Multipipe Product	Integrated Circuit Supplier	Integrated Circuit	GPU Core	Configuration

2. Respondent MediaTek's Accused Products

Table No. 3: Accused MediaTek Singlepipe Product

Accused MediaTek Singlepipe Product	GPU	Configuration	RTL Version	Driver Version

Table No. 4: Accused MediaTek Multipipe Products

Accused MediaTek Multipipe Product	GPU	Configuration	RTL Version	Driver Version

Accused MediaTek Multipipe Product	GPU	Configuration	RTL Version	Driver Version

3. Respondent SDI's Accused Products

Table No. 5: SDI Accused Multipipe Products

Accused SDI Multipipe Product	Part Number	GPU	Configuration	RTL Version	Driver Version

Accused SDI Multipipe Product	Part Number	GPU	Configuration	RTL Version	Driver Version

[2] This is the part number identified in Appendix A of Complainants' Pre-Hearing. Based on the naming convention of all the other SDI part numbers, it is possible that Complainants inadvertently omitted a letter, which I have indicated with an underscore, so that the correct part number would read, [ ], with the appropriate letter inserted in place of the underscore.

Accused SDI Multipipe Product	Part Number	GPU	Configuration	RTL Version	Driver Version

Inv. No. 337-TA-1044
App. B to ID
April 13, 2018

APPENDIX B: DI PRODUCTS[1]

Table No. 1: Complainants' Single Shader Products

Single Shader Product	GPU Core	Configuration	Practiced '506 Patent Claims	Practiced '133 Patent Claims
Bristol Ridge	GFX8	1 Shader Engine	1 and 8	1, 3, 8
Carrizo	GFX8	1 Shader Engine	1 and 8	1, 3, 8
Iceland	GFX8	1 Shader Engine	1 and 8	1, 3, 8
Stoney Ridge	GFX8.1	1 Shader Engine	1 and 8	1, 3, 8
Raven Ridge	GFX9	1 Shader Engine	1 and 8	1, 3, 8

Table No. 1: Complainants' Multi Shader Products

Multi Shader Product	GPU Core	Configuration	Practiced '506 Patent Claims	Practiced '133 Patent Claims
Polaris 11 (Baffin)	GFX8	2 Shader Engines	1-5, 8	1, 3, 8
Polaris 12	GFX8	2 Shader Engines	1-5, 8	1, 3, 8
Fiji	GFX8	4 Shader Engines	1-5, 8	1, 3, 8
Polaris 10 (Ellesmere)	GFX8	4 Shader Engines	1-5, 8	1, 3, 8
Polaris 22	GFX8	4 Shader Engines	1-5, 8	1, 3, 8
Tonga	GFX8	4 Shader Engines	1-5, 8	1, 3, 8
Vega 10	GFX9	4 Shader Engines	1-5, 8	1, 3, 8
Vega 12	GFX9	4 Shader Engines	1-5, 8	1, 3, 8

[1] The information contained in these tables was taken from Appendix A of Complainants' Pre-Hearing Brief.

Multi Shader Product	GPU Core	Configuration	Practiced '506 Patent Claims	Practiced '133 Patent Claims
Vega 20	GFX9	4 Shader Engines	1-5, 8	1, 3, 8

CERTAIN GRAPHICS SYSTEMS, COMPONENTS THEREOF, AND CONSUMER PRODUCTS CONTAINING THE SAME

Inv. No. 337-TA-1044

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **INITIAL DETERMINATION** has been served by hand upon the Commission Investigative Attorney, Yoncha L. Kundupoglu, Esq., and the following parties as indicated, on **May 10, 2018**.

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
Washington, DC 20436

On Behalf of Complainants:

Michael T. Renaud, Esq.
MINTZ LEVIN COHN FERRIS GLOVSKY AND POPEO P.C.
One Financial Center
Boston, MA 02111

☐ Via Hand Delivery
☒ Via Express Delivery
☐ Via First Class Mail
☐ Other:_____

On Behalf of Respondents VIZIO, Inc.:

Cono A. Carrano
AKIN GUMP STRAUSS HAUER & FELD, LLP
Robert S. Strauss Building
1333 New Hampshire Avenue, NW
Washington, DC 20036

☐ Via Hand Delivery
☒ Via Express Delivery
☐ Via First Class Mail
☐ Other:_____

On Behalf of Respondents MediaTek, Inc., MediaTek USA Inc., and Sigma Designs, Inc.:

Tyler T. VanHoutan
McGuireWoods LLP
600 Travis Street, Suite 7500
Houston, Texas 77002

☐ Via Hand Delivery
☒ Via Express Delivery
☐ Via First Class Mail
☐ Other:_____